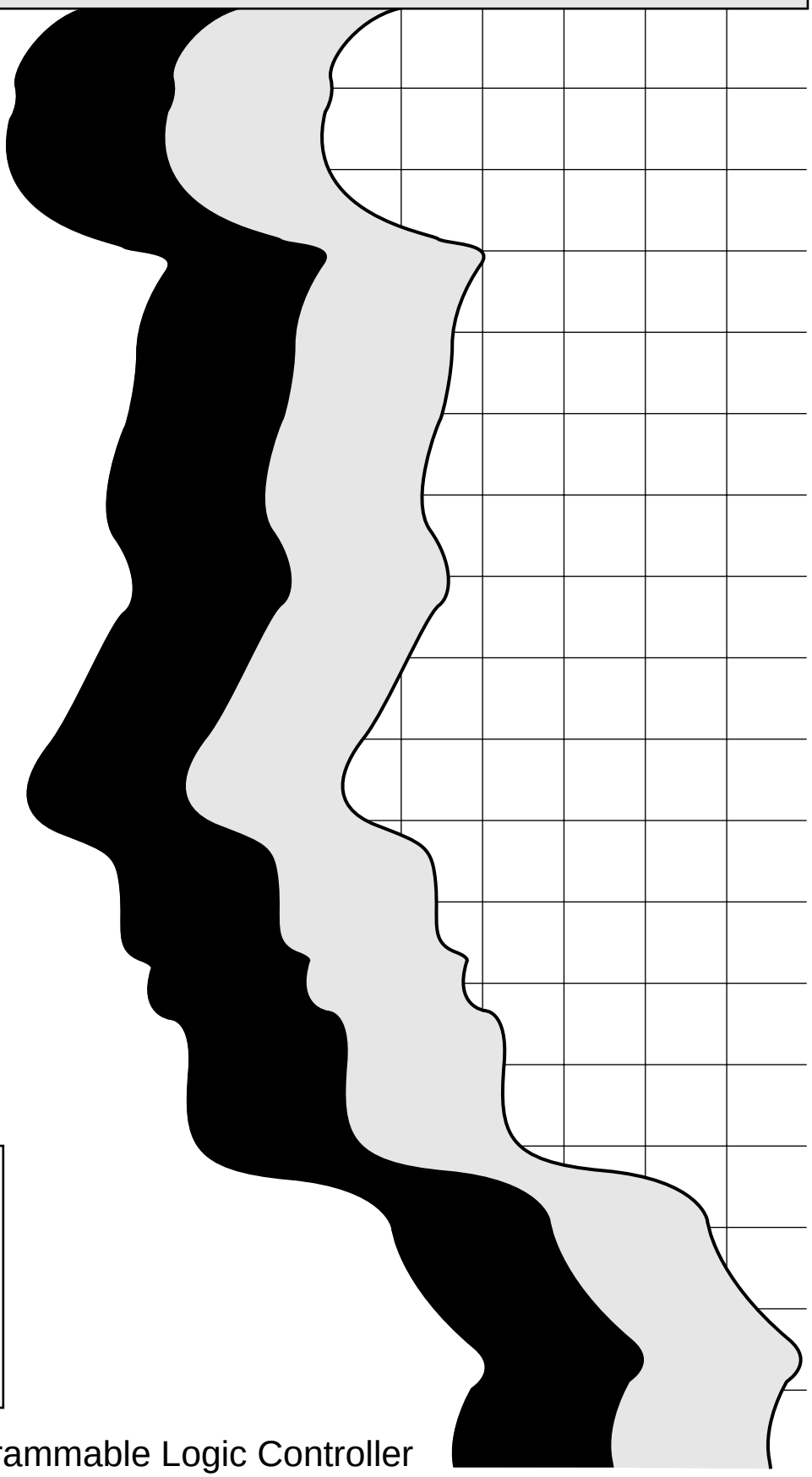
MITSUBISHI

High Speed Counting Module Type AD61C

User's Manual



MELSEC

Mitsubishi Programmable Logic Controller

• SAFETY PRECAUTIONS •

(Always read before starting use.)

Before using this product, please read this manual introduced in this manual carefully and pay full attention to safety to handle the product correctly.
The instructions given in this manual are concerned with this product. For the safety instructions of the programmable controller system, please read the user's manual for the CPU module to use.
In this manual, the safety instructions are ranked as "DANGER" and "CAUTION".

⚠ DANGER	Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.
⚠ CAUTION	Indicates that incorrect handling may cause hazardous conditions, resulting in medium or slight personal injury or physical damage.

Note that the ⚠CAUTION level may lead to a serious consequence according to the circumstances. Always follow the instructions of both levels because they are important to personal safety.

Please store this manual in a safe place and make it accessible when required. Always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- Do not write data into the "system area" of the buffer memory of intelligent function modules. Writing data into the "system area" may cause a PLC system malfunction.
- Depending on the malfunction of the external output transistor, there may be cases where the output is ON or OFF status. Install external monitoring circuitry for output signals that may lead to major accidents.

⚠ CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other.
  They should be installed 150 mm(5.9 inch) or more from each other.
  Not doing so could result in noise that may cause malfunction.

[INSTALLATION PRECAUTIONS]

⚠ CAUTION

- Securely fix the module with a DIN rail or mounting screws, and securely tighten the mounting screws in the specified torque range.
- Loose tightening can cause a drop, short circuit or malfunction.
  Overtightening can cause a drop, short circuit or malfunction due to damage to the screws and module.
- Switch all phases of the external power supply off when mounting or removing the module.
  Not ding so may cause electric shock or damage to the module.
- Do not directly touch the conductive area or electronic components of the module.
  Doing so may cause malfunction or failure in the module.

[WIRING PRECAUTIONS]

⚠ CAUTION

- Perform correct pressure-displacement, crimp-contact or soldering for connector wire connections using the tools specified by the manufactures.
  Attach connectors to the module securely.
- Be careful not to let foreign matters such as sawdust or wire chips get inside the module.
  They may cause fires, failure or malfunction.
- The top surface of the module is covered with protective film to prevent foreign objects such as cable offcuts from entering the module when wiring.
  Do not remove this film until the wiring is complete.
  Before operating the system, be sure to remove the film to provide adequate heat ventilation.
- Be sure to fix communication cables or power supply cables leading from the module by placing them in the duct or clamping them.
  Cables not placed in the duct or without clamping may hang or shift, allowing them to be accidentally pulled, which may cause a module malfunction and cable damage.
- When removing the communication cable from the module, do not pull the cable. When removing the cable with a connector, hold the connector on the side that is connected to the modules.
  Pulling the cable that is still connected to the module may cause malfunction or damage to the module or cable.

[WIRING PRECAUTIONS]

⚠ CAUTION

- Always ground the shielded cable on the encoder side (relay box).
  Otherwise, malfunction may occur.
- When wiring, be sure to verify the rated voltage of the product as well as the terminal layout. Fire or failure may result if incorrect voltage is input or incorrect wiring is performed.
- Connecting terminals with incorrect voltage may result in malfunction or mechanical failure.

[STARTUP/MAINTENANCE PRECAUTIONS]

⚠ CAUTION

- Do not disassemble or modify the module.
  Doing so could cause failure, malfunction, injury or fire.
- Switch all phases of the external power supply off when mounting or removing the module.
  Not doing so may cause failure or malfunction of the module.
- Do not touch the connector while the power is on.
  Doing so may cause malfunction.
- Switch all phases of the external power supply off when cleaning or retightening the terminal screws and module installation screws.
  Not doing so may cause failure or malfunction of the module.
  If the screws are loose, it may cause the module to fallout, short circuits, or malfunction.
  If the screws are tightened too much, it may cause damages to the screws and/or the module, resulting in the module falling out, short circuits or malfunction.
- Always make sure to touch the grounded metal to discharge the electricity charged in the body, etc., before touching the module.
  Failure to do so may cause a failure or malfunctions of the module.

[DISPOSAL PRECAUTIONS]

⚠ CAUTION

- When disposing of the product, handle it as industrial waste.

REVISIONS

※The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
May, 1990	IB (NA) 66246-A	First edition
Nov., 2004	IB (NA) 66246-B	Partial Correction Chapter 1,Section 1.1, 2.1, 2.2, 2.3, 2.5, Chapter 3, Section 3.6, 4.2.2, 4.3, 4.4, 4.5, 4.5.1, 4.5.2, 4.5.3, 4.5.5, 4.5.6, 4.5.7, Chapter 5, Section 5.1.1, 5.1.2, 5.1.3, 5.2.1, 5.2.2, 5.2.3, 5.2.4, 5.3, 5.3.1, Section 5.3.2, 5.4.1, 5.4.2, 5.5, 5.5.1, 5.5.2, 5.5.3, 5.5.5, 5.5.6, 5.5.7, Chapter 6, Section 6.1.1, 6.1.2, 6.1.3, 6.2.1, 6.2.2, 6.2.3, 6.2.4, 6.3.1, 6.3.2, 6.4.2, 6.5, Section 6.5.1, 6.5.2, 7.1, 7.2, 7.4.1, 7.5.2, 7.5.3, 8.1, 8.5 Addition SAFETY PRECAUTIONS, WARRANTY

Japanese Manual Version IB-68181-E

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

1. GENERAL INTRODUCTION ..... 1-1~1-3

1.1 Features 1-2

2. SPECIFICATIONS ..... 2-1~2-6

2.1 General Specifications 2-1
2.2 Performance Specifications 2-2
2.3 Cable Specifications 2-3
2.4 Function List 2-4
2.5 Interface with External Equipment 2-5
2.6 Connectable Encoders 2-6

3. COUNTER PROCESSING METHOD ..... 3-1~3-8

3.1 Counting at 1-Phase Pulse Input 3-2
3.2 Counting at 2-Phase Pulse Input 3-3
3.3 Counter Value's Comparison Signal Output Processing 3-4
3.3.1 Counter value's coincidence/magnitude comparison signals output 3-4
3.3.2 Counter value coincidence signal external output 3-5
3.4 Preset (Initial Value Setting) Function 3-6
3.5 Ring Counter Function 3-7
3.6 Count Start/Stop Processing by External Input 3-8

4. LINKING TO THE A2CCPU ..... 4-1~4-20

4.1 System Configuration 4-1
4.1.1 Overall configuration 4-1
4.1.2 Cautions on constructing the system 4-2
4.2 Data Communication Processing 4-3
4.2.1 Communication method 4-3
4.2.2 Processing time 4-4
4.3 I/O Signals To/From the PC CPU 4-5
4.4 Buffer Memory Assignment 4-7
4.5 Programming 4-9
4.5.1 Basic programs 4-9
4.5.2 Example 1-phase/2-phase input counting programs 4-10
4.5.3 Example program for setting set value and preset value data 4-13
4.5.4 Example preset program by external input 4-15
4.5.5 Example program of counter present value preset 4-16
4.5.6 Example program of ring counter function 4-18
4.5.7 Programs when 2 channels are used 4-20

5. HOW TO LINK AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU AND MINI -S3 MASTER MODULE ..... 5-1~5-31

5.1 System Configuration 5-1
5.1.1 Overall configuration 5-1
5.1.2 Applicable system 5-2
5.1.3 Cautions on constructing the system 5-3
5.2 Data Communication Processing 5-4
5.2.1 Communication method 5-4
5.2.2 I/O signal processing 5-5
5.2.3 Buffer memory data processing 5-6
5.2.4 Processing time 5-7
5.3 I/O Signals to/from PLC CPU 5-8
5.3.1 AD61C I/O signals 5-8
5.3.2 MINI -S3 master module I/O signals 5-10
5.4 Buffer Memory Assignment 5-11
5.4.1 AD61C buffer memory 5-11
5.4.2 MINI -S3 master module buffer memory 5-13
5.5 Programming 5-15
5.5.1 Basic programs 5-15
5.5.2 Example 1-phase/2-phase input counting programs 5-20
5.5.3 Example program for setting set value and preset value data 5-24
5.5.4 Example preset program by external input 5-26
5.5.5 Example program of counter present value preset 5-27
5.5.6 Example program of ring counter function 5-29
5.5.7 Programs when 2 channels are used 5-31

6. ACPU AND MINI -S3 MASTER MODULE LINK ..... 6-1~6-32

6.1 System Configuration 6-1
6.1.1 Overall configuration 6-1
6.1.2 Applicable system 6-2
6.1.3 Cautions on constructing the system 6-3
6.2 Data Communication Processing 6-4
6.2.1 Communication method 6-4
6.2.2 I/O signal processing 6-5
6.2.3 Buffer memory data processing 6-6
6.2.4 Processing time 6-7
6.3 I/O Signals to the Sequencer CPU 6-8
6.3.1 AD61C I/O signals 6-8
6.3.2 MINI -S3 master module I/O signals 6-10
6.4 Buffer Memory Assignment 6-11
6.4.1 AD61C buffer memory 6-11
6.4.2 MINI -S3 master module buffer memory 6-13
6.5 Programming 6-15
6.5.1 Basic programs 6-15
6.5.2 Example 1-phase/2-phase input counting programs 6-20
6.5.3 Example program for setting set value and preset value data 6-24
6.5.4 Example preset program by external input 6-27
6.5.5 Example program of counter present value preset 6-28
6.5.6 Example program of ring counter function 6-30
6.5.7 Programs when 2 channels are used 6-32

7. INSTALLATION AND PRE-OPERATION SETTING PROCEDURES ..... 7-1~7-12

7.1 Pre-operation Setting Procedures 7-1
7.2 Handling Precautions 7-2
7.3 Nomenclature 7-3
7.4 Settings 7-5
7.4.1 Station number settings 7-5
7.4.2 Ring counter settings 7-5
7.5 Mounting Procedures 7-6
7.5.1 Mounting directions 7-6
7.5.2 DIN rail adapter 7-6
7.5.3 Mounting to the DIN rail 7-7
7.6 Wiring of Data Link Cables 7-8
7.6.1 Handling instructions for twisted pair cables 7-8
7.6.2 Link cable connections 7-8
7.7 Connecting External Devices 7-9
7.7.1 Wiring instructions 7-9
7.7.2 Wiring example for the connection with the open collector output pulse generator 7-10
7.7.3 Voltage output pulse generator and wiring examples 7-11
7.7.4 Wiring example for the connection of a controller to external input terminals (DIS, PRST) 7-12
7.7.5 Wiring examples at external output (EQU) terminal 7-12

8. TROUBLESHOOTING ..... 8-1~8-4

8.1 Error Code List 8-1
8.2 RUN LED is Flickering/OFF 8-2
8.3 LINK RUN LED is OFF 8-2
8.4 LINK ERR. LED is ON 8-2
8.5 Count Operations Do Not Execute 8-3
8.6 Count Value is Incorrect 8-4

APPENDICES ..... APP-1~APP-2

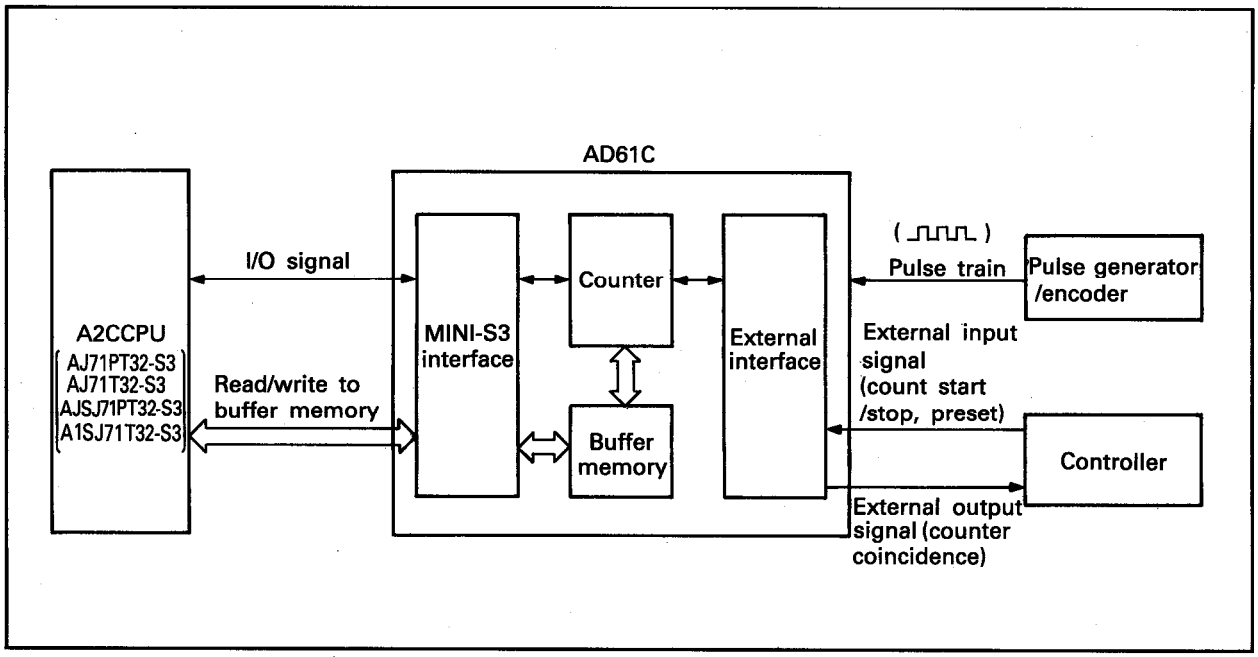
APPENDIX 1 Dimensions APP-1
APPENDIX 2 DIN Adapter Dimensions APP-2

1. GENERAL INTRODUCTION

This manual describes the specifications, handling instructions, and programming information for the AD61C high speed counting module (hereafter referred to as AD61C). The AD61C configures data link with the A2CCPU or the AJ71PT32-S3 AJ71T32-S3 A1SJ71PT32-S, A1SJ71T32-S3 MELSECNET/MINI S3 master module using twisted pair cables to execute high speed counting of up to 50 kpps.

The AD61C is used for counting 1- and 2-phase pulse inputs as follows.
1-phase pulse input ····· 2 counts/input pulse.
2-phase pulse input ····· 4 counts/input pulse of phases A and B.

General operations for the AD61C are shown below.



(1) There are 2 channels for 1- and 2-phase pulse input terminals.

(2) The AD61C starts, stops and presets (count initial value setting) counting by the sequence program or by an external input signal.

(3) The magnitude comparison of the counter value between the CPU and the AD61C and the counter preset value are read by the sequence program and sequence processing can be executed.

(4) When the increment/decrement count value and the set value coincide, the AD61C outputs the coincidence signal to the sequence program or to an external terminal.

(5) High speed automatic preset can be executed using the ring counter function.

1.1 Features

(1) A maximum of 14 AD61C modules can be connected.
Using twisted pair cables, a maximum of 14 AD61C modules can be connected at intervals of 100 m (328.1 ft) or less.

(2) A maximum counting speed of 50 kpps is possible for 1- and 2-phase pulse input signals.
A 1-phase input pulse rise (leading edge)/fall (trailing edge) registers 2 counts and the rise/fall of each phase of a 2-phase input pulse registers 4 counts. The maximum speed for both 1- and 2-phase pulse inputs is 50 kpps.

(3) Preset, ring count
(a) Preset value write rewrites the counter present value in a 24-bit range (0 to 16,777,215) to an optional value. Preset can be executed by the sequence program or by an external input.
(b) By setting the ring counter switch, the coincidence signal is output when the counter value becomes equal to the set value. Since the preset value is simultaneously preset automatically, counting can be repeated.

(4) The counter coincidence signal can be output an external device.
Since the coincidence signal is output to the external terminal of the AD61C at the same time the counter coincidence or the magnitude comparison signal is output to the PC CPU, external control is possible.

(5) Count start/stop by external input is possible.
With the external input (disable input) OFF, after the sequence program turns the counter start signal ON and counting has started, applying voltage to the external input terminal (disable terminal) stops the counting. Thus, counting can be started and stopped by turning the external input terminal OFF/ON.

(6) Mounting to the DIN rail.
The AD61C can be mounted to the DIN rail using a special adapter.

In this User's Manual, the modules are generally referred to as follows:

A2CCPU	A2CJCPU A2CCPU(P21/R21) A2CCPU-DC24V A2CCPUC24(-PRF)
ACPU	A1SJ(H),A1S(H),A2S(H),A2US(H),Q2AS(H)CPU A1N,A2N,A2N-S1,A3NCPU(P21(S3)/R21) A1,A2,A2-S1,A3CPU(P21/R21) A3HCPU(P21/R21) A3MCPU(P21/R21) A2A,A2A-S1,A3ACPU(P21(S3)/R21) A2U,A2U-S1,A3U,A4UCPU Q2A,Q2A-S1,Q3A,Q4ACPU
A0J2CPU	A0J2CPU(P23/R23),A0J2HCPU(P21/R21)
AnACPU	A2A,A2A-S1,A3ACPU(P21/R21)
AnUCPU	A2US(H),A2U,A2U-S1,A3U,A4UCPU
QnACPU	Q2AS(H),Q2A,Q2A-S1,Q3A,Q4ACPU
MINI-S3 master module	AJ71PT32-S3,AJ71T32-S3 A1SJ71PT32-S3,A1SJ71T32-S3

POINT

AD61C I/O addresses in this manual apply when the AD61C is set as station 01 and remote terminal No. 1, with either the A2CCPU or MINI-S3 master module as the master station.
When the AD61C setting is other than station 01 or remote terminal No. 1, perform programming using the I/O addresses allocated to the AD61C station number (1 station occupies 8 points, AD61C occupies 32 points for 4 stations) and its remote terminal number.

Refer to the following related manuals.

- A2CCPU(P21/R21), A2CCPU-DC24V, A2CCPUC24(-PRF), A2CJCPU User's Manual (Details) SH(NA)-3492
- AJ71PT32-S3, AJ71T32-S3, A1SJ71PT32-S3, A1SJ71T32-S3 MELSECNET/MINI-S3 Master Module User's Manual SH(NA)-3521

2. SPECIFICATIONS

2.1 General Specifications

The general specifications of AD61C are shown in Table 2.1.

<table>
<tr><th>Item</th><th colspan="5">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="5">0 to 55℃</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">−20 to 75℃</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="5">10 to 90% RH, non-condensing</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90% RH, non-condensing</td></tr>
<tr><td rowspan="3">Vibration resistance</td><td rowspan="3">Conforms to * JIS C 0911</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 55 Hz</td><td>——</td><td>0.075 mm (0.003 in)</td><td rowspan="2">10 times
*(1 octave/minute)</td></tr>
<tr><td>55 to 150 Hz</td><td>1 G</td><td>——</td></tr>
<tr><td>Shock resistance</td><td colspan="5">Conforms to JIS C 0912 (10 g × 3 times in 3 directions)</td></tr>
<tr><td>Dielectric withstand voltage</td><td colspan="5">500 VAC for 1 minute across DC external terminals and ground</td></tr>
<tr><td>Insulation resistance</td><td colspan="5">5 MΩ or larger by 500 VDC insulation resistance tester across DC external terminals and ground</td></tr>
<tr><td>Grounding</td><td colspan="5">Class D grounding is not required when it is impossible.</td></tr>
<tr><td>Operating ambience</td><td colspan="5">Free of corrosive gases. Dust should be minimal.</td></tr>
<tr><td>Cooling method</td><td colspan="5">Self-cooling</td></tr>
</table>

Table 2.1 General Specifications

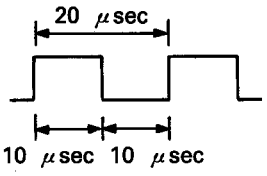
REMARK

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10 Hz to 20 Hz, from 20 Hz to 40 Hz, from 40 Hz to 20 Hz, and 20 Hz to 10 Hz are referred to as one octave.

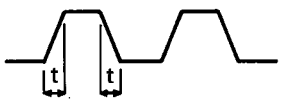
Note: * JIS: Japanese Industrial Standard

2.2 Performance Specifications

The following indicates the performance specifications of the AD61C.

Item			Specifications	
Number of occupied stations (number of occupied points)			4 stations (32 points)	
Number of channels			2 channels	
Performance specifications of 1 channel	Count input signal	Phase	1 phase input, 2 phase input	
		Signal level (Phase A, Phase B)	5 VDC / 12 VDC / 24 VDC } 2 to 5 mA	(For input voltage and operating current guaranteed value, refer to Section 3.7)
	Counter	Counting speed *(Maximum)	1 phase input	50 KPPS
			2 phase input	50 KPPS
		Counting range	24 bits binary 0 to 16,777,215 (decimal)	
		From	Increment/decrement preset counter plus ring counter function	
		Minimum count pulse width (1-, 2-phase inputs)	 Rise time and fall time of input should be 5 μsec or less each. Duty ratio: 50%	
	Magnitude comparison between CPU and AD61C	Comparison range	24 bits, binary	
		Comparison result	Set value ≦ count value Set Value = count value Set value > count value	
	External input	Preset	12/24 VDC, 3/6 mA 5 VDC, 5 mA	
		Count disable	12/24 VDC, 3/6 mA 5 VDC, 5 mA	
	External output	Coincidence output	Transistor (open collector) output 12/24 VDC, 0.3 A	
Maximum transmission distance between stations			50 (twisted pair cable 0.3 mm² (164.05 ft)) 100 (twisted pair cable 0.5 mm² (328.1 ft)) } Unlimited total distance	
24 VDC internal current consumption (A)			0.15	
External dimensions (mm)			170 (6.69) × 100 (3.94) × 80 (3.15)	
Weight kg (lb)			1.0 (2.2)	

* : (1) The pulse rise/fall time determines whether the counting speed is correct or incorrect. Countable pulse inputs are as follows.



(For both 1 and 2 phase inputs)
t = 5 μs ····· 50 KPPS
t = 50 μs ····· 5 KPPS

(2) If a pulse input has a rise/fall time greater than t = 50 μsec, the AD61C may miscount and cannot be used.

2.3 Cable Specifications

Cables which can be used with the AD61C are as follows.

(1) 5-core flat cable cut wiresThese cables, used when the AD61C is installed adjacently to the A2CCPU or A2CCPU I/O module, can transmit data while supplying 24 VDC. Cable specifications are given below.

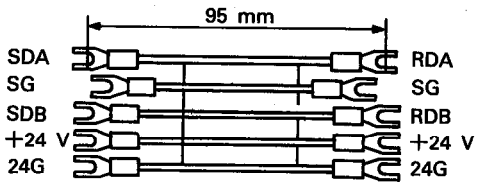
Model	A2C-005	A2C-C007
Module intervals	0 to 34 mm	0 to 54 mm
Conductor resistance	0.2 Ω	
Insulation resistance (20℃)	15 MΩkm or larger	
Dielectric withstand voltage V-min	200 VAC	
Cable length	53±9mm	73±9mm
Configuration		

Table 2.3 5-core Flat Cable Specifications

(2) Twisted pair cable

Item	Specifications
Cable type	Shielded twisted pair cable
Logarithm	2P or larger
Conductor resistance (20℃)	88.0 Ω/km or less
Electrostatic capacity (1 kHz)	Average 60 nF/km or less
Characteristic impedance (100 kHz)	110 ± 10 Ω

Table 2.5 Twisted pair Cable Specifications

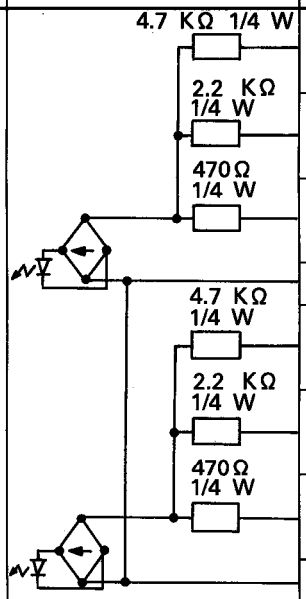
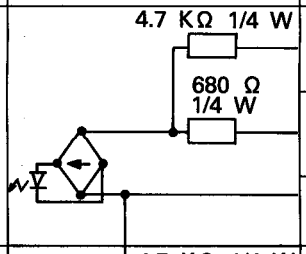
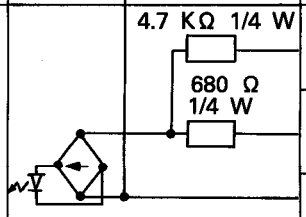
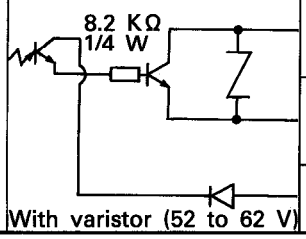
2.4 Function List

Functions of the AD61C are as follows.

No.	Function	Content	Refer to
1	Count function at 1-, 2-phase pulse inputs	• Receives a 1- or 2-phase pulse and counts the rise and fall of each. A 1-phase input registers 2 counts/input pulse. A 2-phase input registers 4 counts/input pulse of phases A and B. • Specifies increment/decrement count to the buffer memory at 1-phase input. At 2-phase input, automatically judges the sum when phase A leads phase B pulse, and the difference when phase B leads phase A.	3.1 3.2
2	Comparison signal output function of the counter	• Compares the counter value and set value and outputs the magnitude (>, <) and coincidence (=) signal to the PC CPU. • When the count value and set value coincide, outputs the coincidence signal to the external terminal (EQU) by turning ON the coincidence signal output enable flag in advance via the sequence program.	3.3
3	Preset function	• Changes the counter present value to a specified value. • Executes preset by the sequence program or by an external preset input.	3.4
4	Ring counter function	• Outputs the coincidence signal when the counter value and set value coincide with the ring counter switch set ON; sets the present value to the preset value automatically at the same time.	3.5
5	Count start/stop by external input function	• Starts and stops counting by turning the external disable (DIS) terminal OFF/ON.	3.6
6	Hardware reset function	• Initializes the AD61C I/O signals and buffer memory (data clear, default value setting) with the reset switch on the front of the AD61C.	7.3
7	Error detection function	• Stores the contents of the first data error detected when FROM/TO instructions from the PC CPU to the AD61C are executed.	8.1

2.5 Interface with External Equipment

The external equipment interface list of AD61C is indicated below.

I/O Division	Internal Circuit	Terminal Number CH1	Terminal Number CH2	Sinal	Operation	Input Voltage (Guaranteed value)	Operation Current (Guaranteed value)
Input (φA φB)		24 V	24 V	Phase A pulse input 24 V	At ON	21.6 to 26.4 V	2 to 5 mA
					At OFF	5 V or less	0.1 mA or less
		12 V	12 V	Phase A pulse input 12 V	At ON	10.8 to 13.2 V	2 to 5 mA
					At OFF	4 V or less	0.1 mA or less
		5 V	5 V	Phase A pulse input 5 V	At ON	4.5 to 5.5 V	2 to 5 mA
					At OFF	2 V or less	0.1 mA or less
		COM	COM	COM			
		24 V	24 V	Phase B pulse input 24 V	At ON	21.6 to 26.4 V	2 to 5 mA
					At OFF	5 V or less	0.1 mA
		12 V	12 V	Phase B pulse input 12 V	At ON	10.8 to 13.2 V	2 to 5 mA
					At OFF	4 V or less	0.1mA or less
		5 V	5 V	Phase B pulse input 5 V	At ON	4.5 to 5.5 V	2 to 5 mA
					At OFF	2 V or less	0.1 mA or less
		COM	COM	COM			
Input (DIS)		12/24 V	12/24 V	Disable input 12/24 V	At ON	10.2 to 26.4 V	2 to 6 mA
					At OFF	2 V or less	0.1 mA or less
		5 V	5 V	Disable input 5 V	At ON	4.5 to 5.5 V	3.5 to 5.5 mA
					At OFF	1.5 V or less	0.1 mA or less
		COM	COM	COM	Response time	OFF → ON 0.5 ms or less	ON → OFF 3 ms or less
Input (PRST)		12/24 V	12/24 V	Preset input 12/24 V	At ON	10.2 to 26.4 V	2 to 6 mA
					At OFF	2 V or less	0.1 mA or less
		5 V	5 V	Preset input 5 V	At ON	4.5 to 5.5 V	3.5 to 5.5 mA
					At OFF	1.5 V or less	0.1 mA or less
		COM	COM	COM	Response	OFF → ON 0.5 ms or less	ON → OFF 3 ms or less
Output (EQU)	 With varistor (52 to 62 V)	OUT	OUT	EQU Open collector	Operating voltage: 10.2 to 30 V Rated voltage: 0.3 A Maximum rush current: 4 A, 10 ms Maximum voltage drop at ON: 1.5 V at 0.5 A Response time: OFF → ON 0.1 ms or less (Resistor load) ON → OFF 0.1 ms or less		
		0 V	0 V	0 V			
		12/24 V	12/24 V	12/24 V external power input	Input voltage: 10.2 to 30 V Current consumption: 2 to 5 mA		

2.6 Connectable Encoders

(1) The encoders which can be connected to the AD61C are as follows.

- Open corrector encoder
- CMOS output encoder
  (Check that the encoder output voltage meets the AD61C specifications.)

REMARK

The following encoders cannot be used with the AD61C.

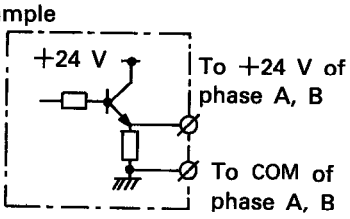
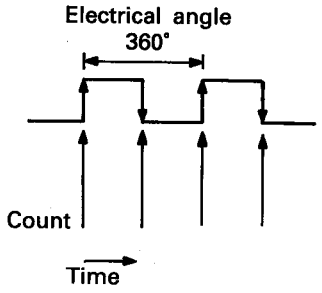
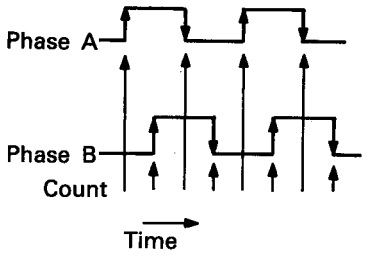
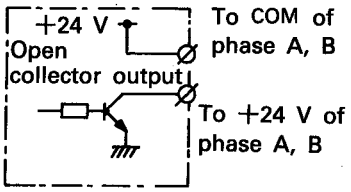
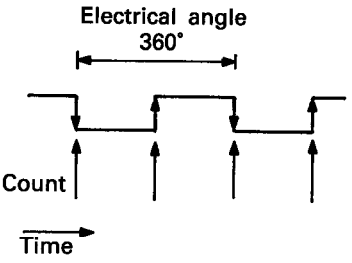
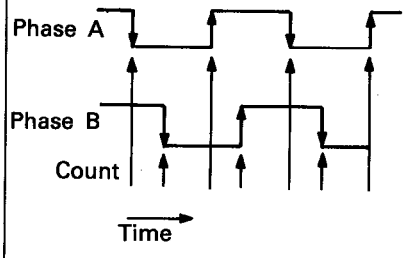
- TTL output encoder
- Line drive output encoder

3. COUNTER PROCESSING METHOD

The AD61C counts 1-phase and 2-phase pulse inputs at rise and fall at a maximum counting speed of 50 kpps.

Both increment and decrement counting are possible in the range of 0 to 16,777,215.

Count timing for 1-phase and 2-phase pulse inputs is shown below for each output type of the pulse generator.

Output Type of Pulse Generator	1-Phase Input	2-Phase Input
Source load (voltage output type) Example 		
Sink load (current output type) Example 		

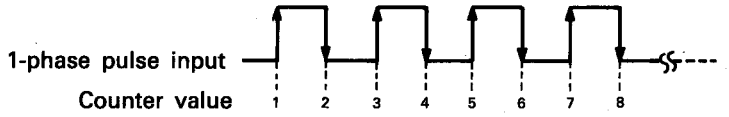
POINT

Explanations in this manual from Section 3 on will be given in reference to source load (voltage output type).

3.1 Counting at 1-Phase Pulse Input

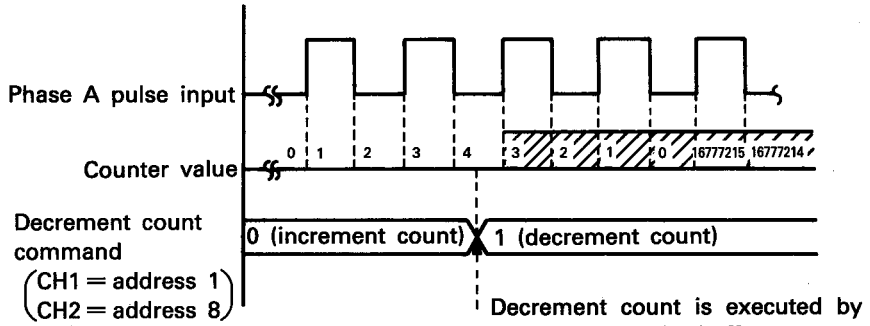
(1) Count method at 1-phase pulse input

a) 1-phase pulse inputs are counted at rise and fall as shown below.



b) The count ratio of pulse inputs is 2.
2 counts are made for 1 pulse input.

(2) Increment/decrement count method
Increment and decrement count timing at 1-phase pulse inputs are shown below.



POINT

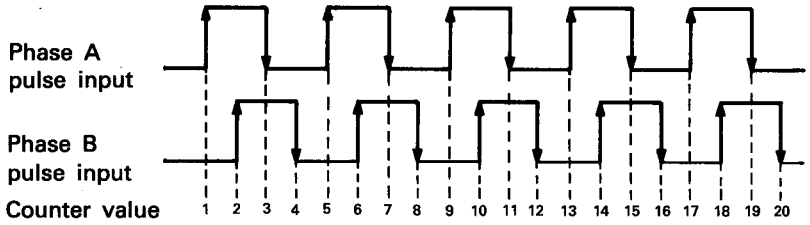
(1) Set pulse inputs so that twice the number of generated pulses is within the counting range 0 through 16,777,215.

(2) Set program set values at twice the required pulse input or at 1/2 the present value (using the 32-bit divide instruction).

3.2 Counting at 2-Phase Pulse Input

(1) Count method at 2-phase pulse input

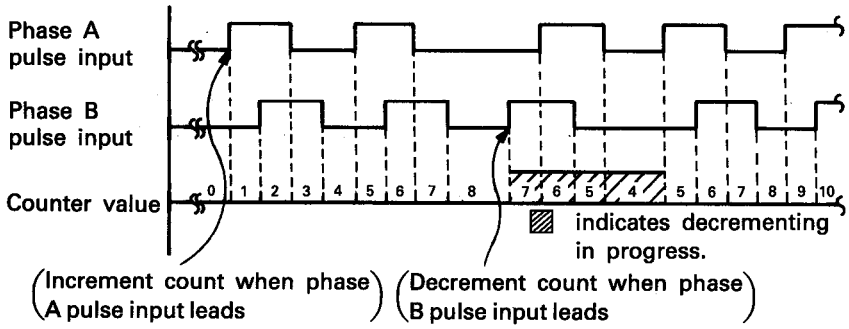
a) Phases A and B of 2-phase pulse inputs are counted at rise and fall as shown below.



b) The count ratio of pulse inputs is 4.
4 counts are made for 1 pulse input of phases A and B.

(2) Increment/decrement count method

Increment and decrement count timing at 2-phase pulse inputs are shown below.



Increment/decrement count is automatically determined according to the relationship between phases A and B as follows.

- Increments when phase A leads phase B
- Decrements when phase B leads phase A

POINT

(1) Set phase A and B pulse inputs so that 4 times the number of generated pulses is within the counting range 0 through 16,777,215.

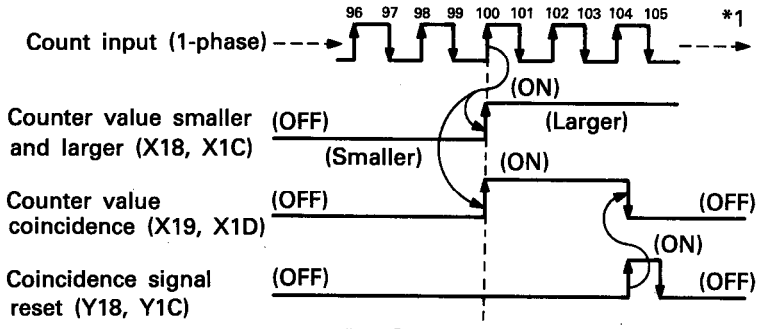
(2) Set program set values at 4 times the required pulse input or at 1/4 the present value (using the 32-bit divide instruction).

3.3 Counter Value's Comparison Signal Output Processing

3.3.1 Counter value's coincidence/magnitude comparison signals output

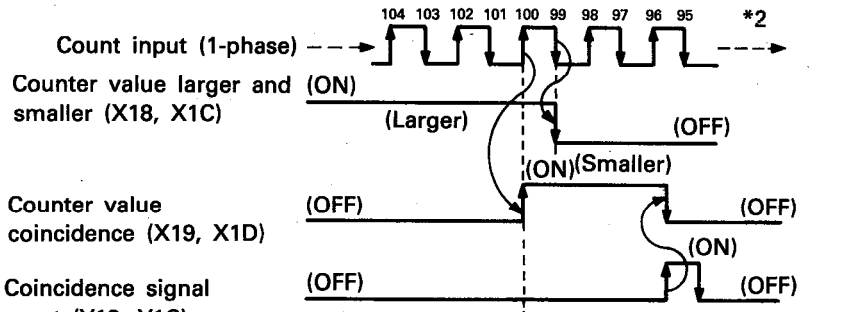
Operation timing for the output of internal I/O comparison signals of the present value and set value are shown below according to increment/decrement count. (I/O numbers are indicated by the assignment numbers of CH1 and CH2 when "01" is the station number of the AD61C.)

(1) Increment count
Increment count when the set value = 100 is shown below.



*1: Count 16,777,215 is followed by 0.

(2) Decrement count
Decrement count when the set value = 100 is shown below.



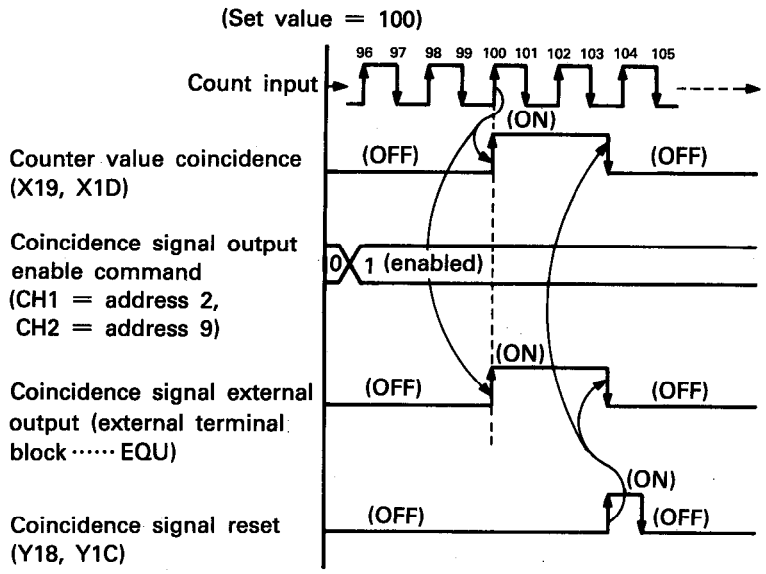
*2: Count 0 is followed by count 16,777,215.

POINT

When the coincidence signal reset (Y18, Y1C) is already turned ON, the counter value coincidence (X19, X1D) will not be latched. If the coincidence signal reset is turned ON, turn it OFF.

3.3.2 Counter value coincidence signal external output

Operation timing for the external output of the counter value coincidence signal is shown below.



(1) The coincidence signal external output is enabled by writing "1" to the buffer memory of the AD61C's coincidence signal output enable flag.

(2) If the counter value and set value coincide, the counter value coincidence signal is turned ON. The coincidence signal external output is output to the external terminal block (EQU) at the same time.

(3) The coincidence signal external output reset is turned OFF by turning ON the coincidence signal reset (Y18, Y1C).

(4) If the coincidence signal reset (Y18, Y1C) is turned ON, turn it OFF. If the coincidence signal reset is ON, the coincidence signal external output will not be latched.

3.4 Preset (Initial Value Setting) Function

The preset function is used to rewrite the counter present value to the initial value (any numeric value). This counter initial value is called the preset value. (For example, when the preset value is 0, counting starts from 0. When the preset value is 100, counting starts from 100.)

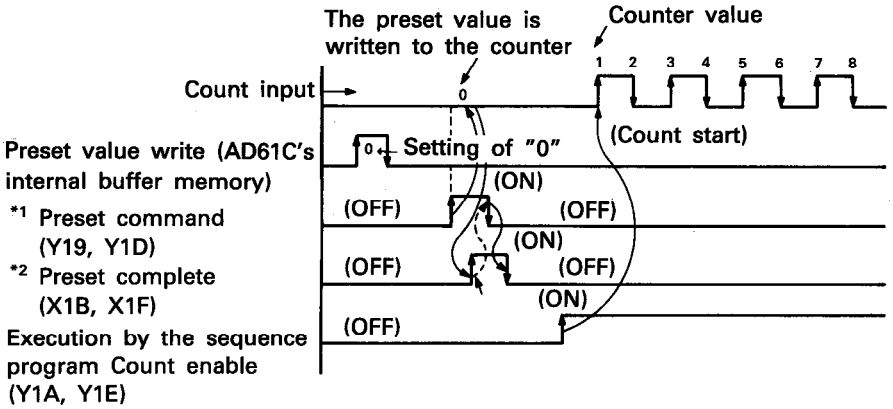
(1) Preset method

a) The preset value is written as a 24-bit binary number to the preset value address (CH1 = 5, 6, CH2 = 12, 13) of the AD61C internal buffer memory using the sequence program.

b) Preset is executed by the sequence program or by external preset input.

Preset Command	Operation
Execution by the sequence program	(1) By turning ON the output signal's preset command (CH1 = Y19, CH2 = Y1D) of the sequence program, the buffer memory's internal preset value is preset to the counter value.
Execution by external preset input	(1) If the preset input is executed to the external terminal (PRST terminal), the preset request detection (CH1 = X1A, CH2 = X1E) is turned ON at the preset input's rise and the buffer memory's internal preset value is preset to the counter value. (2) Because the next external preset input cannot be executed when the preset request detection signal is turned ON, be sure to reset the preset request detection (CH1 = Y1B, CH2 = Y1F) using the sequence program. Even when turned ON, the preset request detection can be reset.

(2) Preset operation timing



*1: Preset when the external input is turned ON. (Turns ON the preset request detection X1A, X1E.)

*2: The preset request detection (Y1B, Y1F) is reset at preset complete (X1B, X1F).

REMARK

For details about reading the counter present value and presetting at the next count, see the sample programs in Sections 4.5.5, 5.5.5, and 6.5.5.

3.5 Ring Counter Function

By setting the ring counter setting switch on the front of the AD61C to ON, if the counter value coincides with the set value, the ring counter function automatically sets the present value to the preset value and executes counter operations. The ring counter function can be used when executing cyclic control such as incremental feed.

(1) Ring counter method

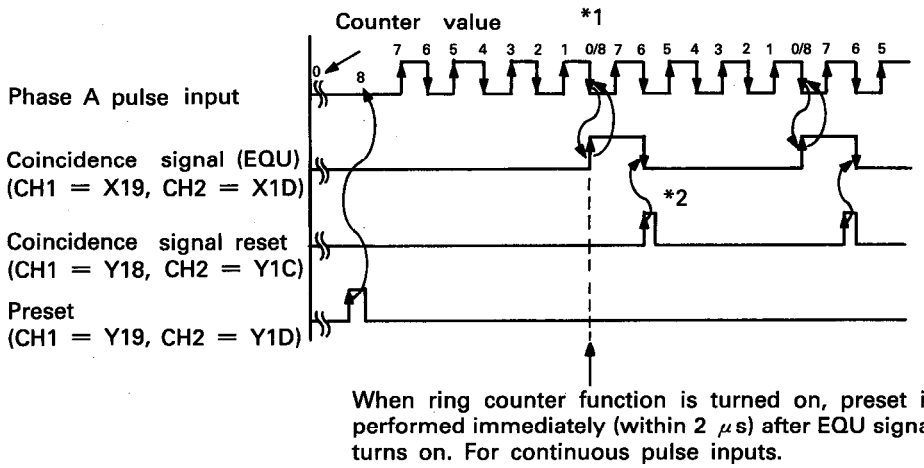
a) Set the ring counter setting switch ON. (See Section 7.4.2 on how to set the switch.)

b) The preset value is written as a 24-bit binary number to the preset value address (CH1 = 5, 6, CH2 = 12, 13) of the AD61C internal buffer memory using the sequence program.

c) The preset value is preset to within 2 μsec if the counter value and set value coincide and the coincidence signal is turned ON. (The preset complete signal (CH1 = X1B, CH2 = X1F) will not operate.)

(2) Ring count operation timing

Set value = 0 Preset value = 8 1 phase down count



When ring counter function is turned on, preset is performed immediately (within 2 μs) after EQU signal turns on. For continuous pulse inputs.

The ring counter performs preset operation internally when the coincidence signal turns on. When preset is executed, counter value is set to 8.

*1 If present value is read at the time of operation, 8 or 0 is read.

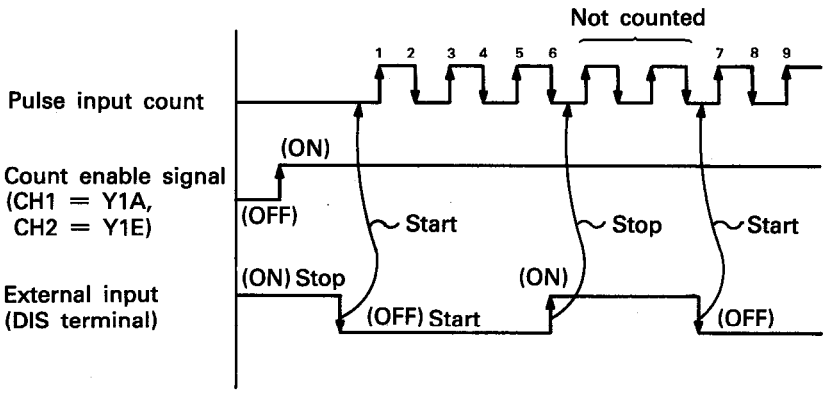
*2 Using the user program, set Y18 and Y1C and reset them. The coincidence signal is reset. If the coincidence signal (X19, X1D) is not turned OFF, the next preset cannot be executed.

3.6 Count Start/Stop Processing by External Input

Count start/stop can be executed regardless of the sequence program's scan time by applying voltage to the external input terminal (disable terminal).

(1) Count start/stop method
   a) Count start is executed by turning the count enable signal (CH1 = Y1A, CH2 = Y1E) ON beforehand using the sequence program and by turning the external input from ON (stop) to OFF (start).
   b) Stop count is executed by turning the external input ON (stop).

(2) Count start/stop operation timing



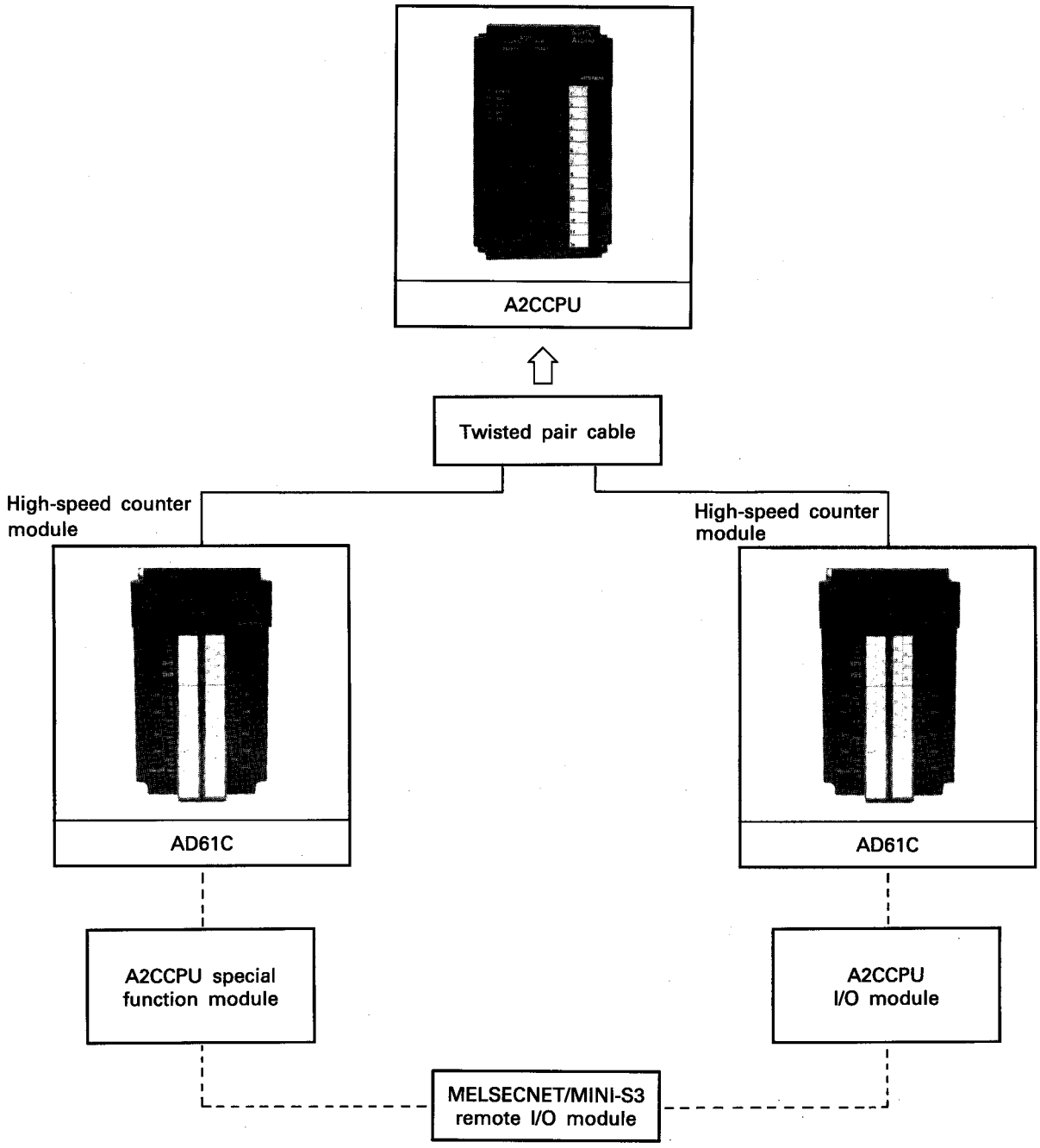
When the count enable signal is turned OFF, count will not be executed even if the external input is turned from ON to OFF.

4. LINKING TO THE A2CCPU

4.1 System Configuration

4.1.1 Overall configuration

(1) The overall configuration of the AD61C using the A2CCPU is shown below.



4.1.2 Cautions on constructing the system

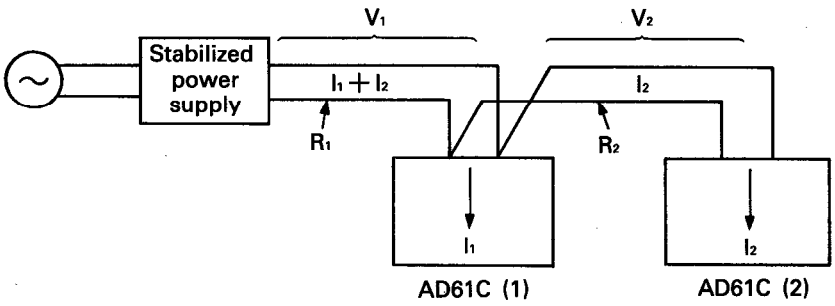
(1) All AD61Cs are linked using twisted pair cables.

(2) Since each AD61C occupies 4 stations and a total of 32 I/O points, be careful when setting station numbers and allocating I/O addresses.

(3) The AD61C requires a 24 VDC power supply.
When supplying power from one power supply to multiple AD61Cs or to the link I/O modules, select proper cables and wiring route taking voltage drops into consideration.

REMARK

Calculating the AD61C's receiving port voltage



V_1 : Voltage drop between stabilized power supply and AD61C (1)
V_2 : Voltage drop between AD61 (1) and AD61C (2)
R_1 : Resistance between stabilized power supply and AD61C (1)
R_2 : Resistance between AD61 (1) and AD61C (2)
I_1 : AD61C (1) current consumption
I_2 : AD61C (2) current consumption

- Calculating voltage drops $V_1 = R_1 \times (I_1 + I_2)$
  $V_2 = R_2 \times I_2$

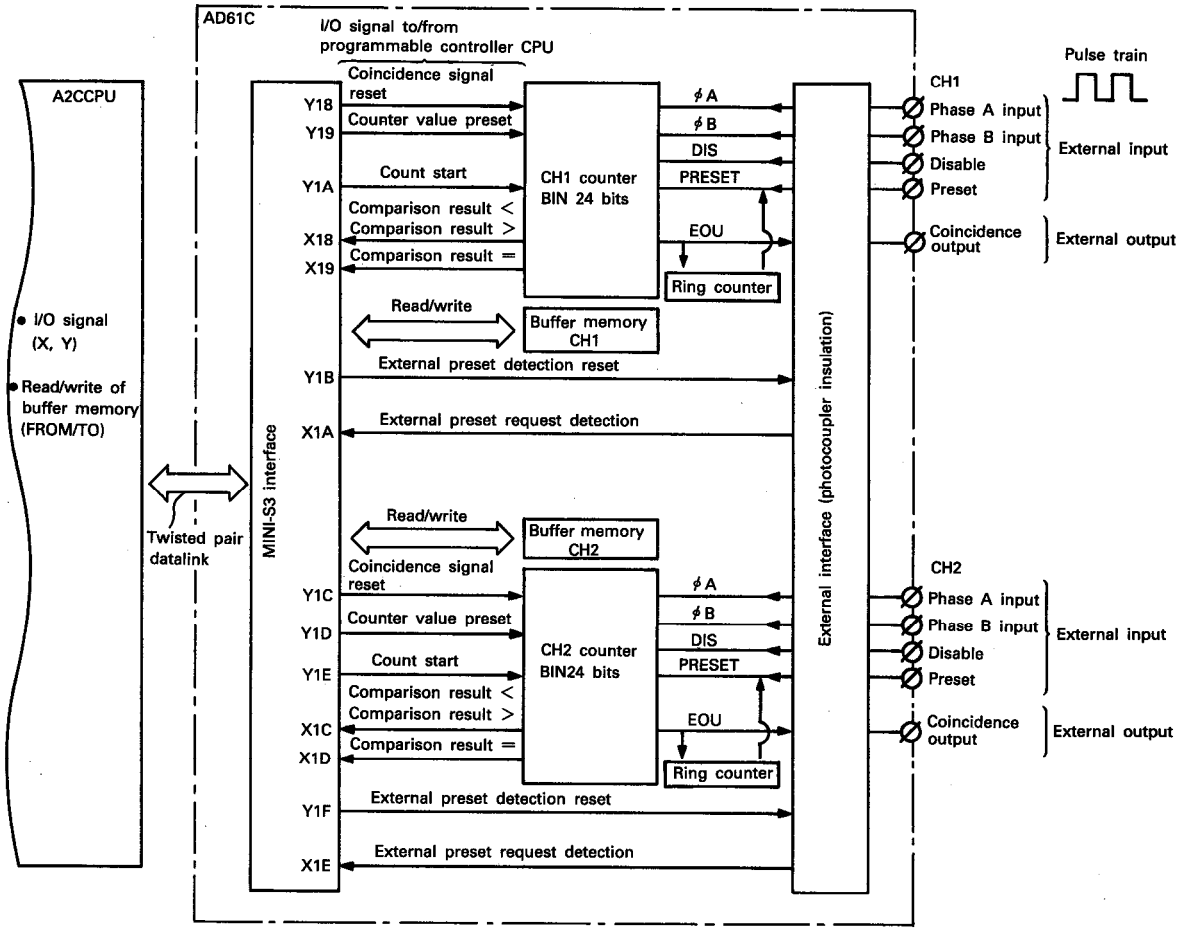
- AD61C's receiving port voltage
  (AD61C (1) receiving port voltage) = (stabilized power supply) − V_1
  (AD61C (2) receiving port voltage) = (stabilized power supply) − ($V_1 + V_2$)

- Connection is possible if the AD61C receiving port voltage is within the range 15.6 V through 31.2 V.

4.2 Data Communication Processing

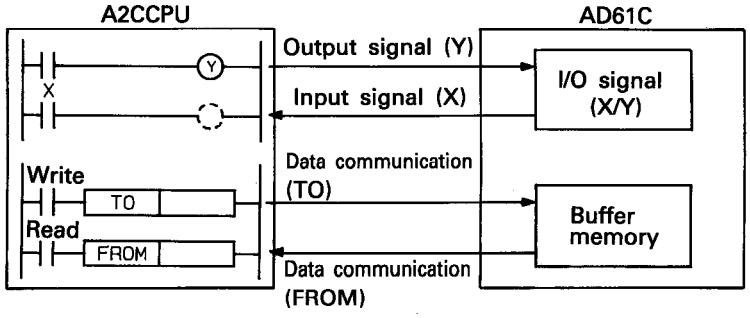
4.2.1 Communication method

(1) Communication between the AD61C and A2CCPU is shown below.



a) The I/O signals and data which indicate the counter run status are transmitted to the A2CCPU via the MINI-S3 interface. Data such as preset value, setting value, and present value are stored in AD61C buffer memory.
b) The same communication processing is executed for both CH1 and CH2.

(2) I/O signal processing and buffer memory data processing are shown below.



a) I/O signal processing

Output (Y): The A2CCPU outputs output signal (Y) to the AD61C at the end processing by turning it ON/OFF using the sequence program.

Input (X): The A2CCPU reads the ON/OFF status of input signal (X) from the AD61C using the sequence program's end processing and executes program operations.

b) Buffer memory data processing

Write: The A2CCPU writes data to the AD61C's buffer memory using the sequence program's TO instruction.

Read: The A2CCPU reads data from the AD61C's buffer memory using the sequence program's FROM instruction.

4.2.2 Processing time

The processing time required to write data to and read data from the AD61C buffer memory is shown below.

(1) Write processing time (T_W)

T_W = (number of data written) × 10 + 90*1 + (A2CCPU scan time) × 2 [ms]

(2) Read processing time (T_R)

T_R = (number of data read) × 10 + 100*1 + (A2CCPU scan time) × 2 [ms]

POINT

(1) Count start/stop by external input, preset, and the counter coincidence signal by external output respond in less than 10 msec.

(2) To increase the processing time responsiveness of sequence operations, use external I/O signals.

REMARK

1) *1: Total value of the A61C internal processing time and the A2CCPU and AD61C system data communication processing time

4.3 I/O Signals To/From the PC CPU

I/O signals to/from the AD61C's A2CCPU are shown below. The I/O device numbers shown here apply when the AD61C's station number is 01 (X/Y00 to X/Y1F).

(1) Input signals (Signal direction: AD61C → A2CCPU)

Device No. CH1	Device No. CH2	Signal	Operation Status
X00 to X03		(Unused)	——
*1 X04		Communication error detection	• Latched at error detection. • If communication error detection reset (Y04) is turned ON, X04 turns OFF.
X05		Reset status detection	• Latched upon AD61C power application or when reset switch is ON. • When reset status detection reset (Y05) is turned ON, X05 turns OFF.
X06		(Unusable)	——
*2 X07		Communication completion wait flag	• Set when data transmission from the A2CCPU Is completed. • Reset when the communication completion wait flag reset signal (Y07) is turned ON, X07turns OFF.
X08 to X17		(Unusable)	——
X18	X1C	CH1/CH2 counter value comparison	• ON: Counter value ≧ set value • OFF: Counter value < set value
X19	X1D	CH1/CH2 counter value coincidence	• Latched if counter value = set value. • When the coincidence signal reset command (Y18, Y1C) is turned ON, X19 and X1D turn OFF.
X1A	X1E	CH1/CH2 external preset request detection	• Latched if an external preset request is given. • When the external preset request detection reset (Y1B, Y1F) is turned ON, X1A and X1E turn OFF.
X1B	X1F	CH1/CH2 preset completion	• Latched at the completion of preset when the preset command (Y19, Y1D) is ON. • When the preset command (Y19, Y1D) is turned OFF, X1B and X1F turns OFF.

*1, *2: Input signals used on the A2CCPU side.

(2) Output signals (Signal direction: A2CCPU → AD61C)

Device No. CH1	Device No. CH2	Signal	Operation Status
Y00 to Y03		(Unused)	———
*1 Y04		Communication error detection reset	• If communication error detection reset (Y04) is turned ON, communication error detection (X04) turns OFF. Error codes of the AD61C buffer memory are reset. • When X04 is OFF, Y05 turns OFF.
Y05		Reset of reset status detection	• When reset status detection reset (Y05) is turned ON, preset status detection (X05) turns OFF. • When X05 is OFF, Y05 turns OFF.
Y06		(Unusable)	———
*2 Y07		Communication completion wait flag reset	• When the communication completion wait flag reset signal (Y07) is turned ON, communication completion wait flag (X07) turns OFF. • When X07 is OFF, Y07 is turns OFF.
Y08 to Y17		(Unusable)	———
Y18	Y1C	CH1/CH2 coincidence signal reset command	• If the coincidence signal reset command (Y18, Y1C) is turned ON, the counter coincidence signal (X19, X1D) and the external output (EQU) turn OFF. • When X19 and X1D are OFF, Y18 and Y1C turn OFF.
Y19	Y1D	CH1/CH2 preset command	• At the rising edge from OFF to ON (_┌‾) of the preset command (Y19, Y1D), the preset value is written. • At the completion of preset (X1B, X1F), Y19 and Y1D turn OFF.
Y1A	Y1E	CH1/CH2 count enable	• When count enable (Y1A, Y1E) is turned ON, counting is enabled. • When count enable (Y1A, Y1E) is turned OFF, counting is disabled.
Y1B	Y1F	CH1/CH2 external preset request detection reset	• When external preset request detection reset (Y1B, Y1F) is turned ON, external preset request detection (X1A, X1E) turns OFF. • When X1A and X1E are OFF, Y1B and Y1F turn OFF.

*1, *2: Output signals used on the A2CCPU side.

4.4 Buffer Memory Assignment

The AD61C can send data to and receive data from the A2CCPU via a buffer memory (without battery backup). When power is turned OFF or when the AD61C is reset, the buffer memory's FROM/TO areas will be cleared (initialized).
When the A2CCPU is reset, the coincidence signal output enable flag of CH1, CH2 (CH1 = 2, CH2 = 9) will be set to the initial value.

Memory buffer assignment is shown below.

Address (decimal)	Name	Description	Read/Write (FROM/TO)	Initial Value
0	CH1 mode register	• 1 or 2-phase input specification • See (1) for data to be specified.	TO (FROM)	18
1	CH1 operation count specification	• Increment/decrement specification • See (2) for data to be specified.	TO	0
2	CH1 coincidence signal output enable flag	• Specification when coincidence signal is output to outside • See (3) for data to be specified.	TO	0
3	CH1 set value	• Storage of higher and middle digit data of set value	TO (FROM)	
4		• Storage of lower digit data of set value		
5	CH1 preset value	• Storage of higher and middle digit data of preset value	TO	0
6		• Storage of lower digit data of preset value		
7	CH2 mode register	• 1 or 2-phase input specification • See (1) for data to be specified.	TO (FROM)	18
8	CH2 operation count specification	• Increment/decrement specification • See (2) for data to be specified.	TO	0
9	CH2 coincidence signal output enable flag	• Specification when coincidence signal is output to outside • See (3) for data to be specified.	TO	0
10	CH2 set value	• Storage of higher and middle digit data of set value	TO (FROM)	
11		• Storage of lower digit data of set value		
12	CH2 preset value	• Storage of higher and middle digit data of preset value	TO	0
13		• Storage of lower digit data of preset value		
14	CH1 present value	• Storage of higher and middle digit data of present value	FROM	
15		• Storage of lower digit data of present value		
16	CH2 present value	• Storage of higher and middle digit data of present value		
17		• Storage of lower digit data of present value		
18	Error code	• Storage of the error code of the first error		

(1) Mode register's written data (CH1 = 0, CH2 = 7)

	Written Data	Initial Value
Used by 1-phase	8	18 (2-phase)
Used by 2-phase	18	

(Caution)
If data other than 8, 18 are written, an error occurs. The error code will be set to address 18 and counting controlled by the initial value.

(2) Decrement count command's written data (CH1 = 1, CH2 = 8)
Valid only for 1-phase inputs.

	Written Data	Initial Value
Decrement count specification	1	0 (increment)
Increment count specification	0	

(Caution)
Written data are valid only for the lower 1 bit. The upper 15 bits will be ignored.

(3) Coincidence signal output enable flag's written data (CH1 = 2, CH2 = 9)

	Written Data	Initial Value
Enable	1	0 (disabled)
Disable	0	

(Caution)
Written data are valid only for the lower 1 bit. The upper 15 bits will be ignored.

POINT

Since increment/decrement count of phases A and B of a 2-phase input will automatically be determined, the contents of the buffer memory will be invalid.

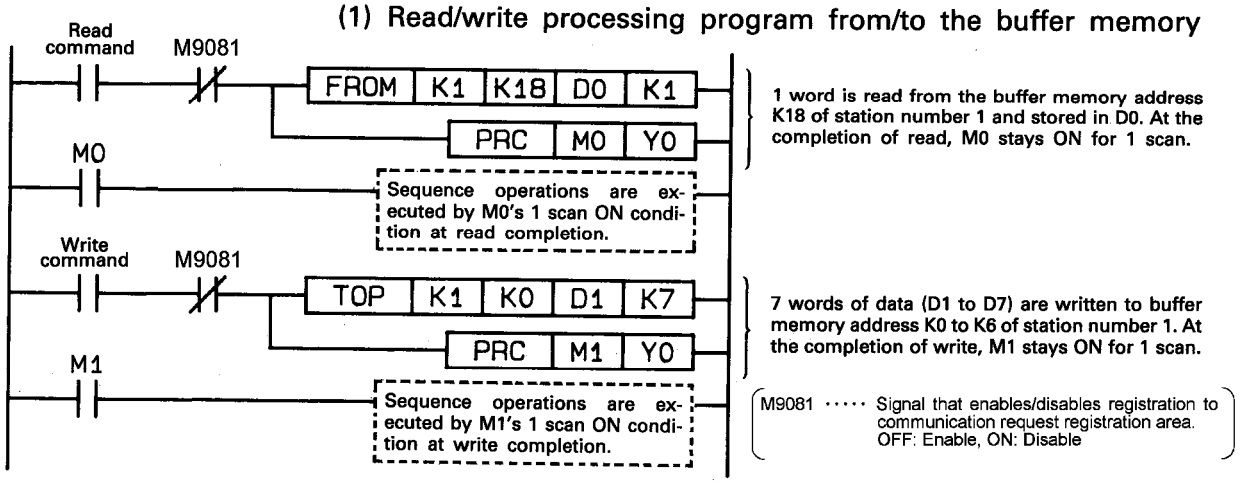
4.5 Programming

Procedures for using sequence program instructions and programming methods will be explained using sample programs.

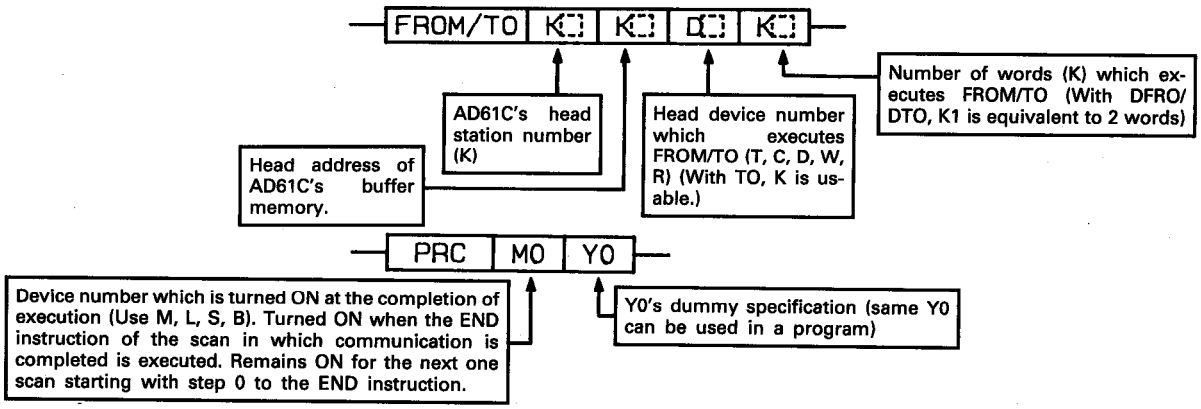
- This program example applies when the remote terminal setting (MINI standard protocol selection) of parameters is performed by the A2CCPU compatible GPP function software package.
- When the A2CCPU compatible GPP function software package is not used, the remote terminal setting of parameters cannot be performed. Therefore, data equivalent to the terminal setting must be written to the special registers by a sequence program. For details, refer to the "A2CCPU(P21/R21), A2CCPU-DC24V, A2CCPUC24(-PRF), A2CJCPU User's Manual" (Details).

4.5.1 Basic programs

(1) Read/write processing program from/to the buffer memory



(2) FROM/TO and PRC instructions
For details, see the ACPU/QnACPU (A mode) Programming Manual (Common Instructions).



POINT

When the FROM/TO instruction is executed by the A2CCPU sequence program, communication is executed via the link. When the PRC instruction execution complete device is turned ON, data communication ends.

4.5.2 Example 1-phase/2-phase input counting programs

(1) Example counting programs for 1-phase and 2-phase inputs are explained below.
- The AD61C's station number is set to 01 (occupying 1 through 4 stations) and the remote terminal (MINI standard protocol) is set by parameter.
- Only CH1's buffer memory is used.
- 1-phase is specified for the pulse input. (The 2-phase setting is entered in the "operation" column below.)
- Decrement count is set.
- The external coincidence signal's output is enabled.
- Preset is not executed by the external input. (Count start/stop can be executed by the external input.)
- The counter present value is not preset.
- The ring counter function is not used.

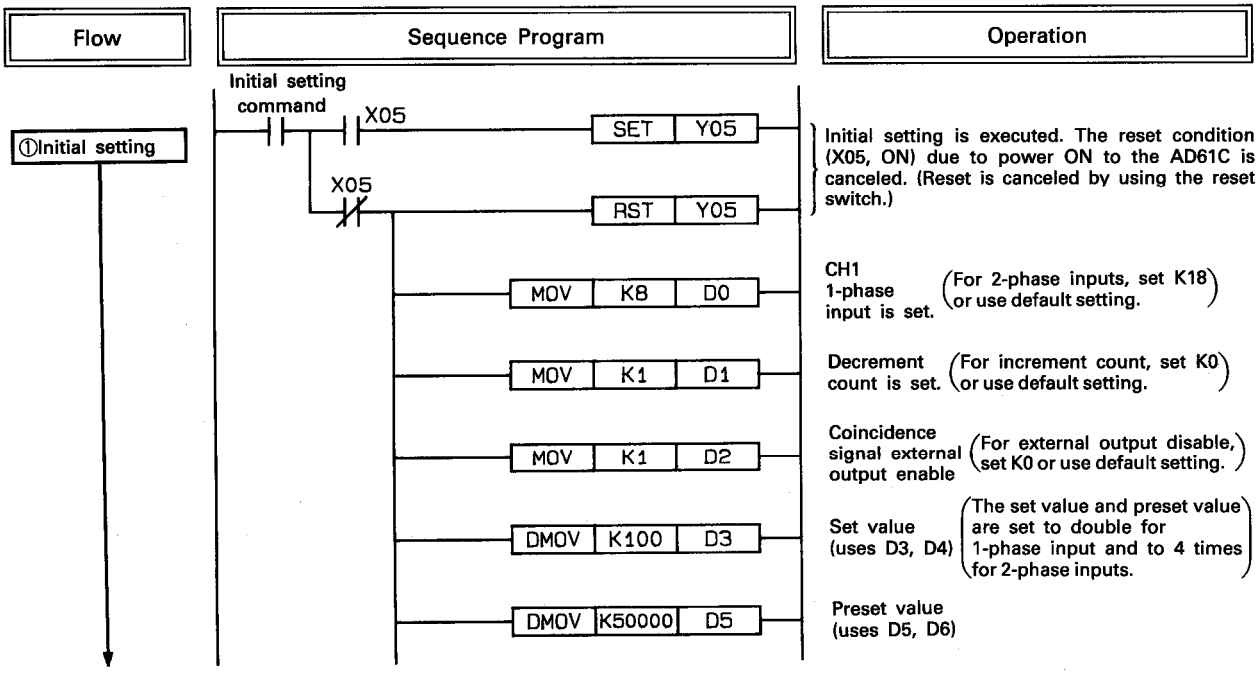
(2) The example program shows the following sequence:
initial setting → coincidence signal reset → preset → count start → coincidence processing → present value and set value read → error code read/reset.

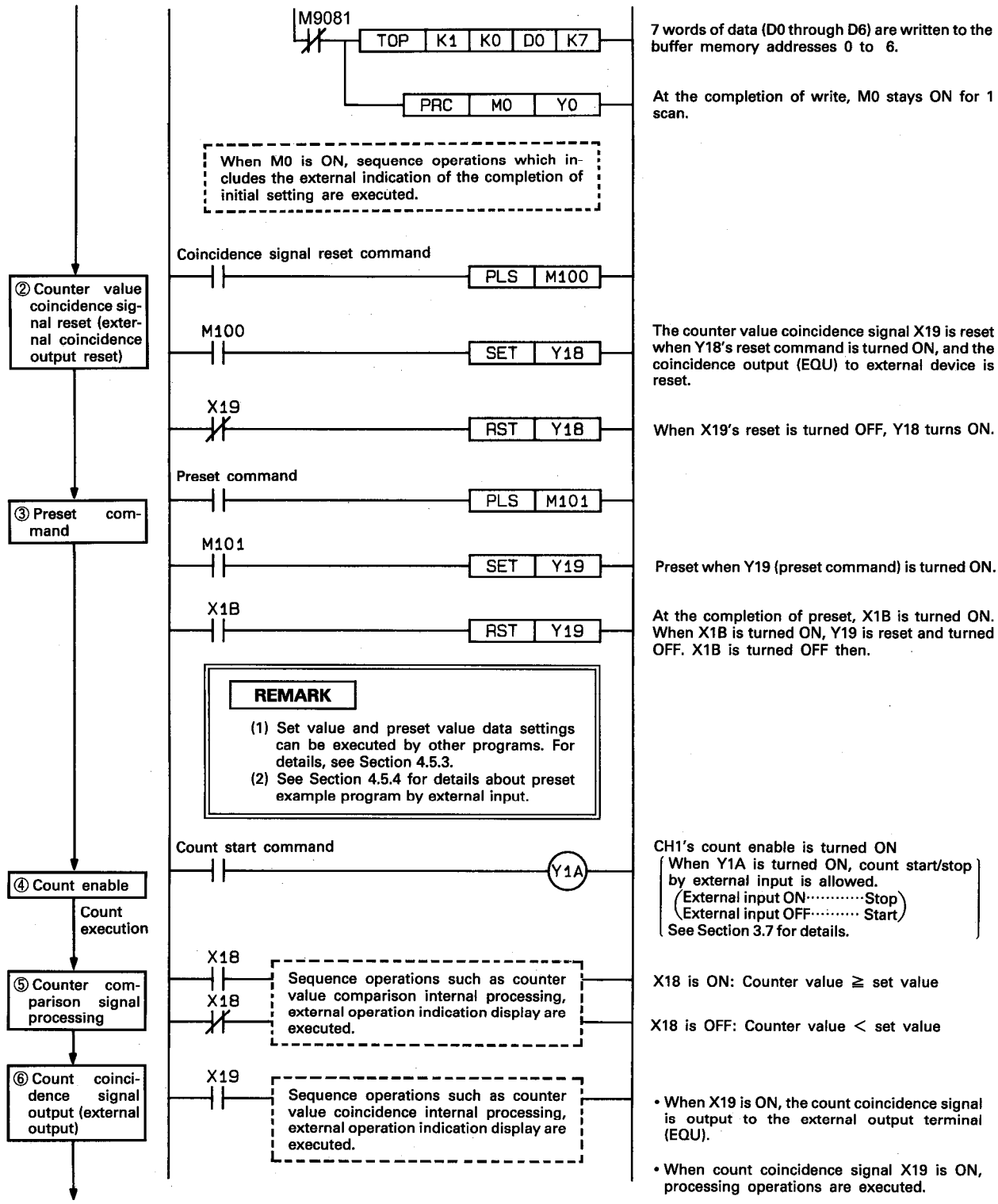
(3) The operation items of the program order are explained in the "flow" column.

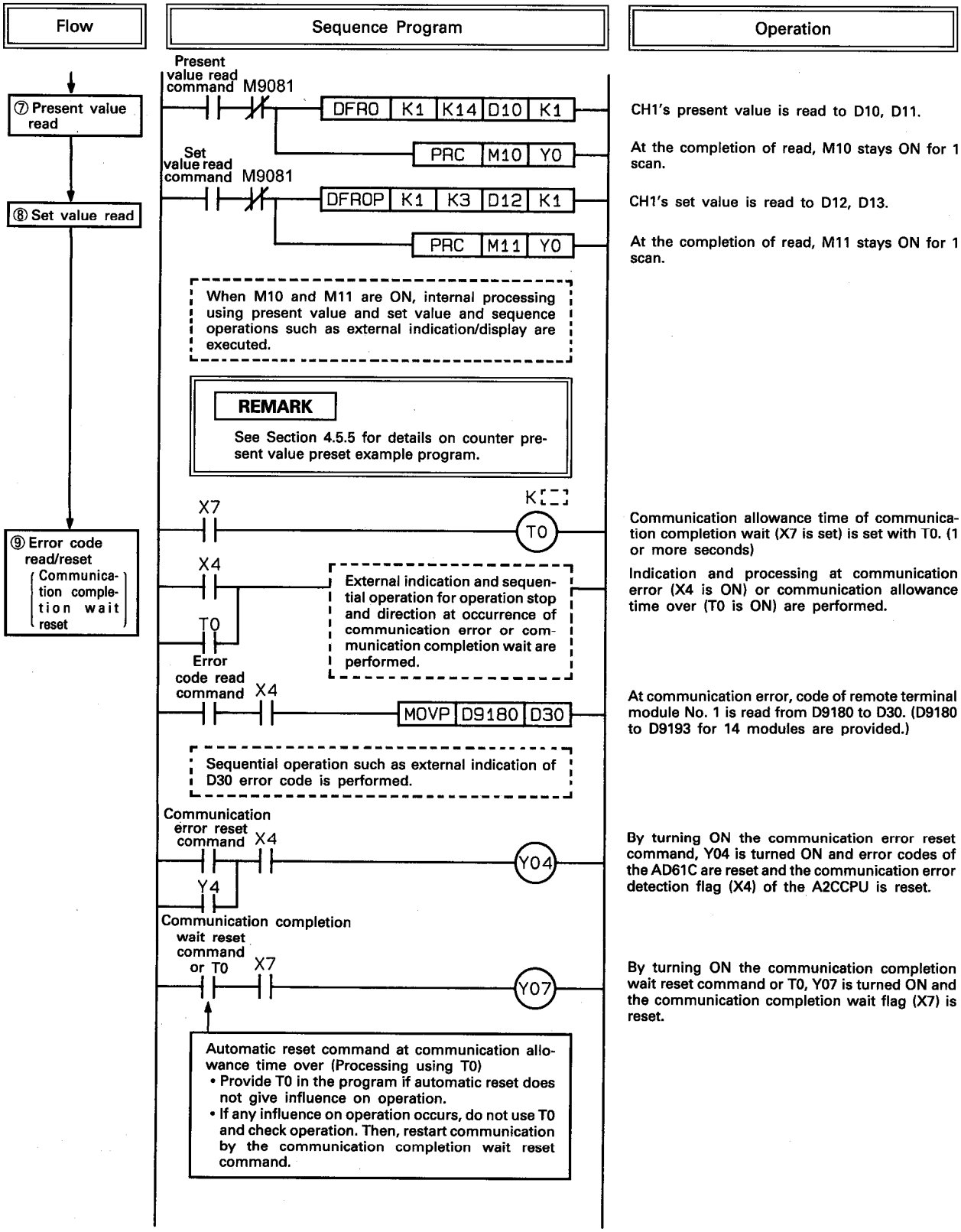
(4) The example program is explained in the "Operation" column.

(5) Initial setting values of the example program are written to the AD61C's buffer memory in batch. (These can also be written to individual addresses one by one.)

(6) Since the AD61C goes to the initial state when the A2CCPU is reset or the AD61C's reset switch is turned ON, execute initial setting again.



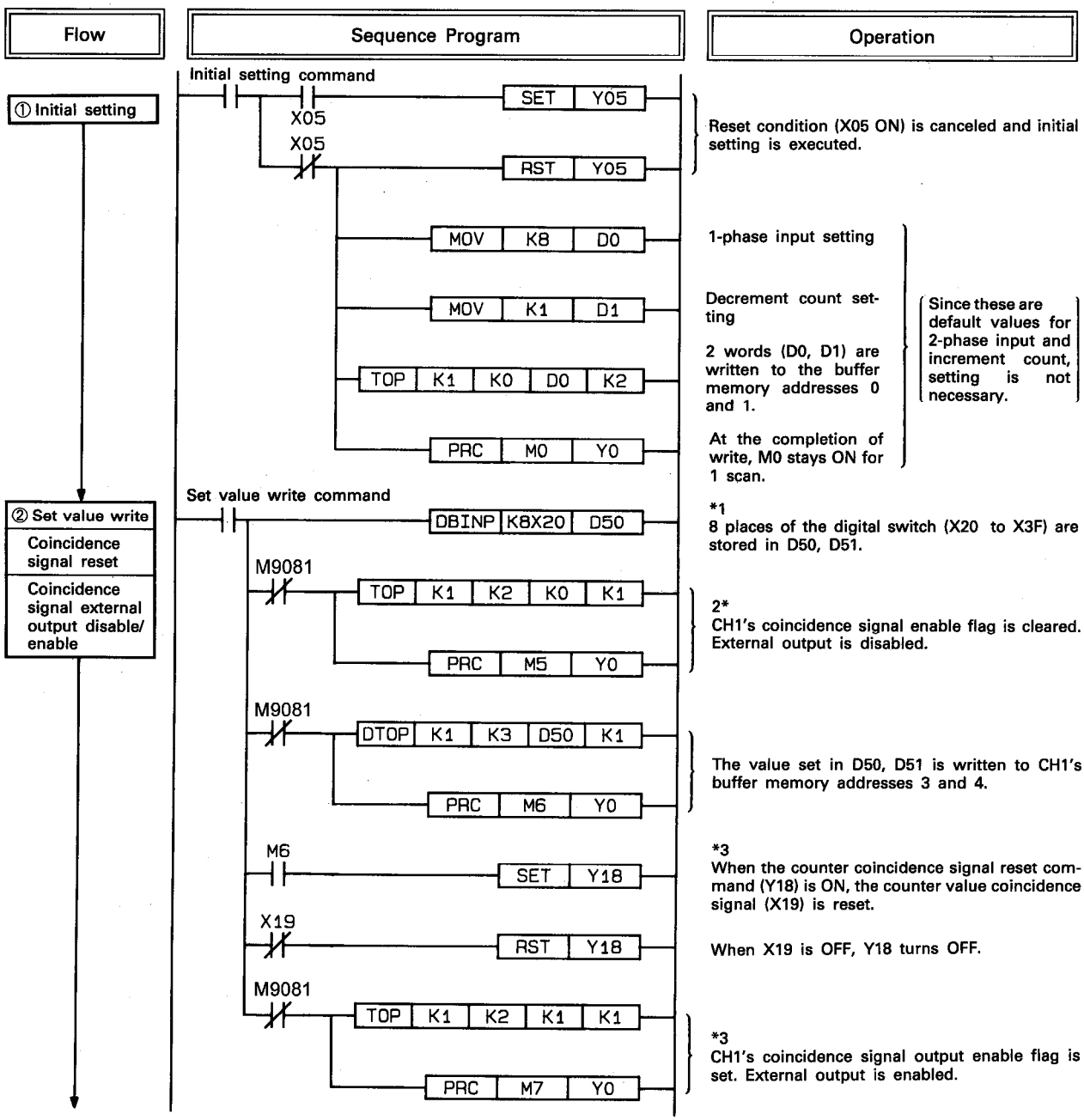

Flow
Sequence Program
Operation
M9081
TOP K1 K0 D0 K7
PRC M0 Y0
7 words of data (D0 through D6) are written to the buffer memory addresses 0 to 6.
At the completion of write, M0 stays ON for 1 scan.
When M0 is ON, sequence operations which includes the external indication of the completion of initial setting are executed.
Coincidence signal reset command
PLS M100
② Counter value coincidence signal reset (external coincidence output reset)
M100
SET Y18
The counter value coincidence signal X19 is reset when Y18's reset command is turned ON, and the coincidence output (EQU) to external device is reset.
X19
RST Y18
When X19's reset is turned OFF, Y18 turns ON.
Preset command
PLS M101
③ Preset command
M101
SET Y19
Preset when Y19 (preset command) is turned ON.
X1B
RST Y19
At the completion of preset, X1B is turned ON. When X1B is turned ON, Y19 is reset and turned OFF. X1B is turned OFF then.
REMARK
(1) Set value and preset value data settings can be executed by other programs. For details, see Section 4.5.3.
(2) See Section 4.5.4 for details about preset example program by external input.
Count start command
Y1A
④ Count enable
Count execution
CH1's count enable is turned ON
When Y1A is turned ON, count start/stop by external input is allowed.
(External input ON····Stop
External input OFF···· Start)
See Section 3.7 for details.
X18
X18
⑤ Counter comparison signal processing
Sequence operations such as counter value comparison internal processing, external operation indication display are executed.
X18 is ON: Counter value ≧ set value
X18 is OFF: Counter value < set value
X19
⑥ Count coincidence signal output (external output)
Sequence operations such as counter value coincidence internal processing, external operation indication display are executed.
• When X19 is ON, the count coincidence signal is output to the external output terminal (EQU).
• When count coincidence signal X19 is ON, processing operations are executed.

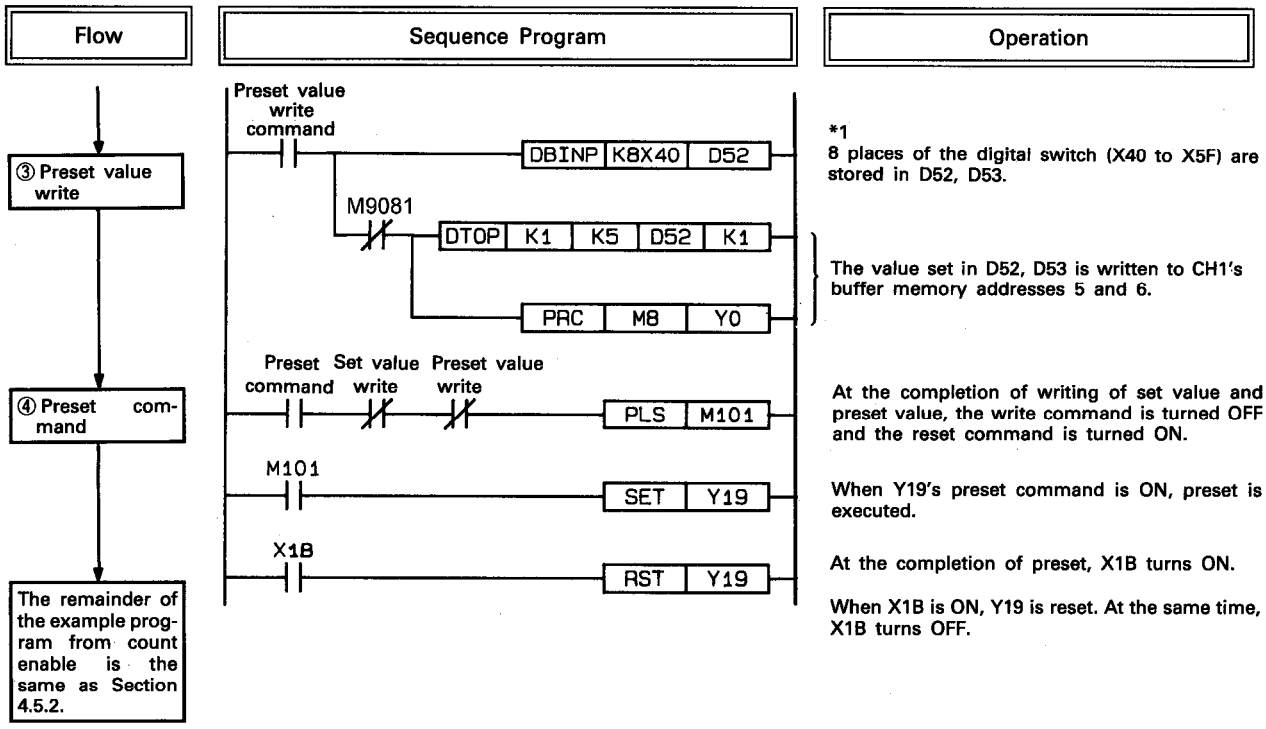

Flow
Sequence Program
Operation
⑦ Present value read
⑧ Set value read
⑨ Error code read/reset (Communication completion wait reset)
Present value read command M9081
DFRO K1 K14 D10 K1
PRC M10 Y0
Set value read command M9081
DFROP K1 K3 D12 K1
PRC M11 Y0
When M10 and M11 are ON, internal processing using present value and set value and sequence operations such as external indication/display are executed.
REMARK
See Section 4.5.5 for details on counter present value preset example program.
X7
K
T0
X4
T0
External indication and sequential operation for operation stop and direction at occurrence of communication error or communication completion wait are performed.
Error code read command X4
MOVP D9180 D30
Sequential operation such as external indication of D30 error code is performed.
Communication error reset command X4
Y4
Y04
Communication completion wait reset command or T0 X7
Y07
Automatic reset command at communication allowance time over (Processing using T0)
• Provide T0 in the program if automatic reset does not give influence on operation.
• If any influence on operation occurs, do not use T0 and check operation. Then, restart communication by the communication completion wait reset command.
CH1's present value is read to D10, D11.
At the completion of read, M10 stays ON for 1 scan.
CH1's set value is read to D12, D13.
At the completion of read, M11 stays ON for 1 scan.
Communication allowance time of communication completion wait (X7 is set) is set with T0. (1 or more seconds)
Indication and processing at communication error (X4 is ON) or communication allowance time over (T0 is ON) are performed.
At communication error, code of remote terminal module No. 1 is read from D9180 to D30. (D9180 to D9193 for 14 modules are provided.)
By turning ON the communication error reset command, Y04 is turned ON and error codes of the AD61C are reset and the communication error detection flag (X4) of the A2CCPU is reset.
By turning ON the communication completion wait reset command or T0, Y07 is turned ON and the communication completion wait flag (X7) is reset.

4.5.3 Example program for setting set value and preset value data

Based on the example sequence program of Section 4.5.2, the example program in which the set value and preset value are fetched by the external digital switch and written to the AD61C is shown.

The necessary program is obtained by replacing sequences from (1) initial setting to (2) preset command of Section 4.5.2 with the following sequences.





*1: Set the set value and preset value to double the number of pulses for 1-phase inputs and to 4 times for 2-phase inputs.

*2: Clear the coincidence signal output enable flag before writing set value. (The counter value and set value might coincide when set value data is being written and therefore the coincidence signal should not be output externally.)

*3: Execute coincidence signal reset after set value write and set the coincidence signal output enable flag.

4.5.4 Example preset program by external input

Based on the example sequence programs of Sections 4.5.2 and 4.5.3, an example program in which the preset command is executed from the external input terminal (PRST terminal) is shown below.

An example program is obtained by replacing
③ preset command program of Section 4.5.2 and
④ preset command program of Section 4.5.3 with the following sequences.

Flow	Sequence Program	Operation
① Preset command (external input)	External preset request detection X1A; Preset complete X1B; SET Y1B; X1A; RST Y1B	When external preset request detection (X1A) and preset completion (X1B) are turned ON by external input, CH1 external preset request detection reset (Y1B) is turned ON and the external preset request detection signal (X1A) is reset. When X1A is OFF, Y1B is reset.

CAUTION

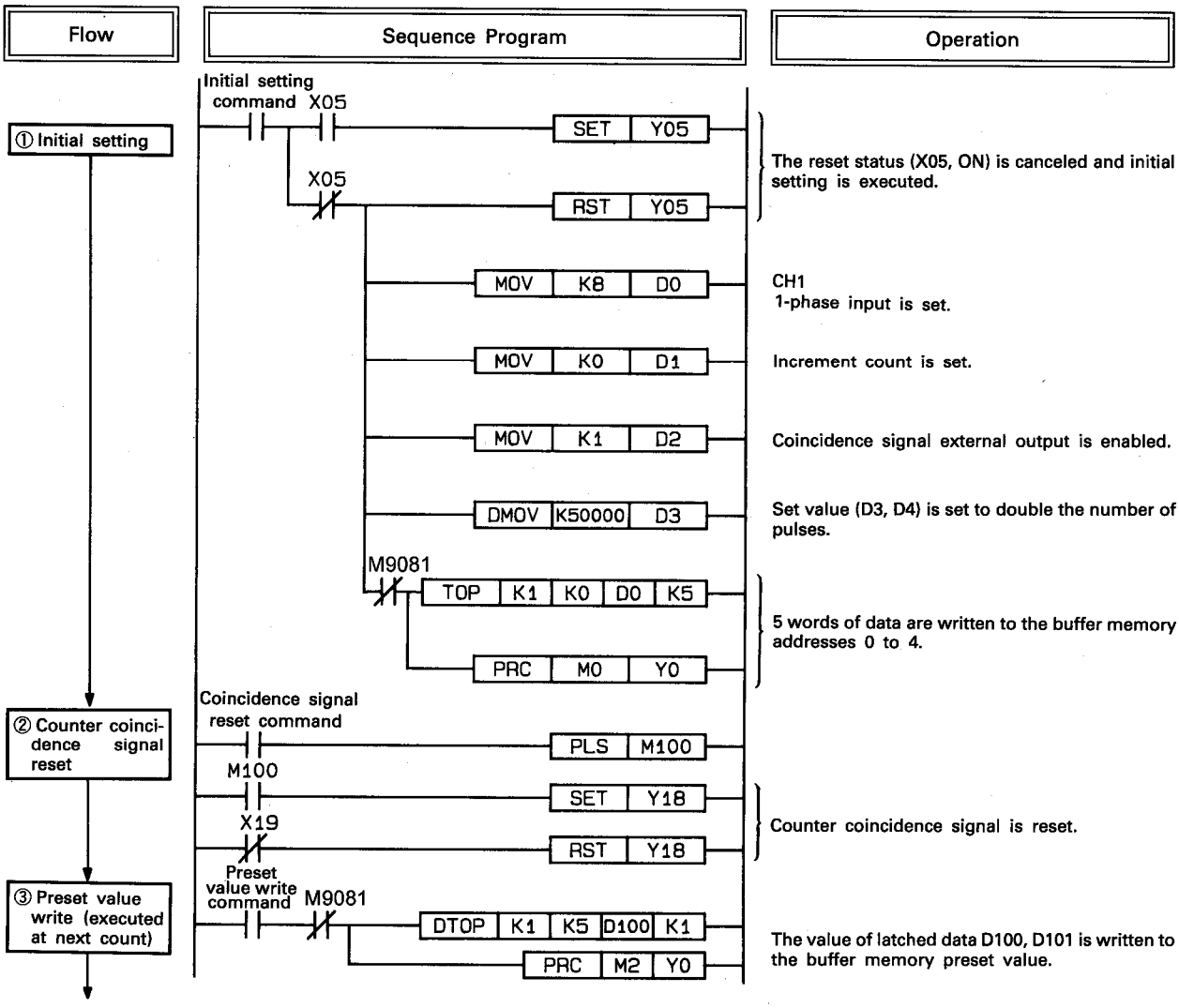
(1) In preset operations by external input, if the preset signal is input to the external terminal (PRST terminal), the external preset request detection (X1A) is turned ON at the preset input's rising edge and the buffer memory internal preset value is preset to the counter value. (See Section 3.4 for details.)
(2) When presetting by external input, reset the external preset request detection each time preset is completed. The next external input is allowed after the external preset request detection is reset.
(3) If the external preset request detection (X1A) is ON, preset by external input and preset command (Y19) by the sequence program cannot operate.
(4) If preset by external input terminal (PRST terminal) is not to be executed, execution of the above program is not necessary.

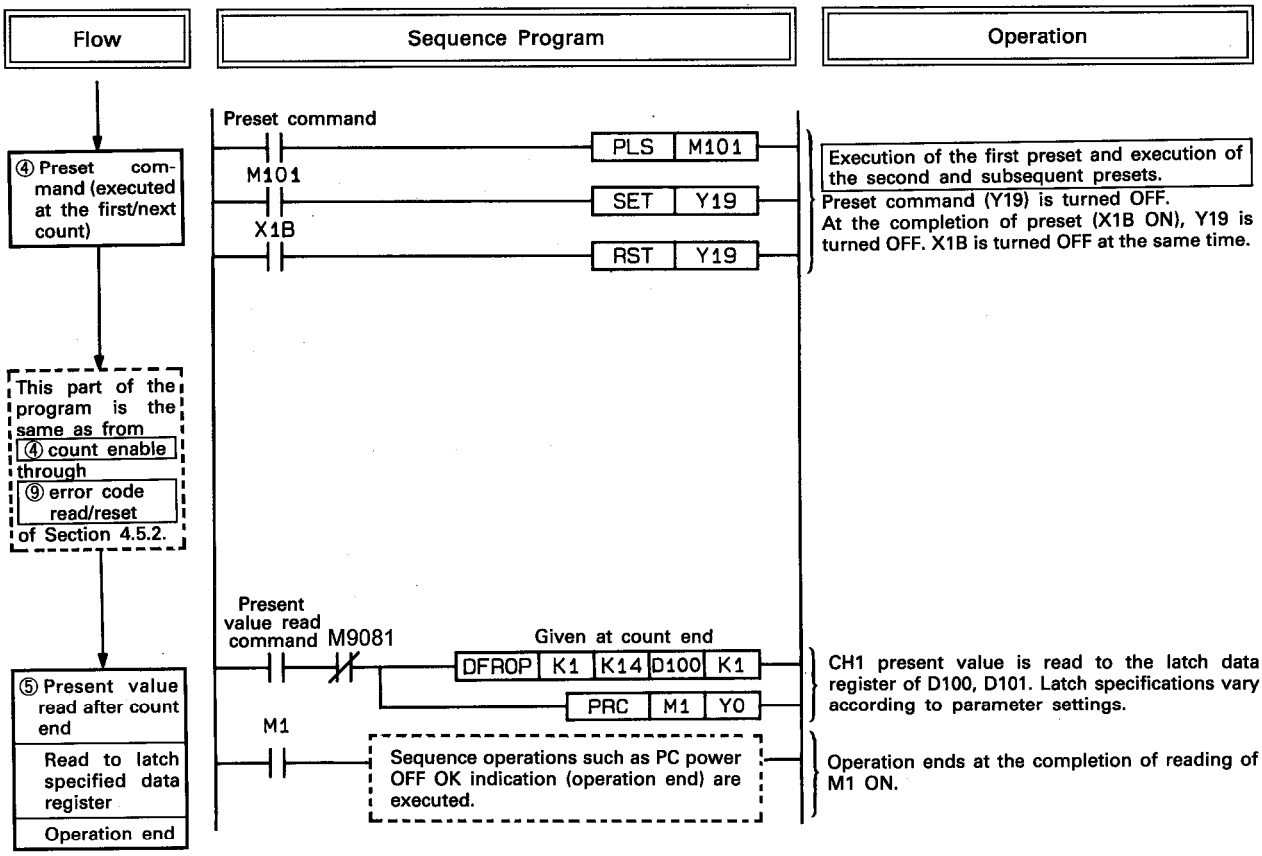
4.5.5 Example program of counter present value preset

An example program in which the counter present value, before the A2CCPU is turned OFF or at count end, is read and counting continues by presetting the read present value before starting the next counting is shown below.

This example program is explained according to the following conditions.

- AD61C station number is set to 01 (occupying 1 to 4 stations).
- CH1 is used.
- 1-phase is specified for the pulse input.
- Increment count is specified.
- The external coincidence signal output is enabled.
- The total number of pulses for the set value is 50,000 (25,000 x 2). The first preset value is 0 (default value).
- The ring counter function is not used.
- Preset is not executed by the external input.
- If the A2CCPU power is turned OFF, the data register which stores the present value is latch specified.



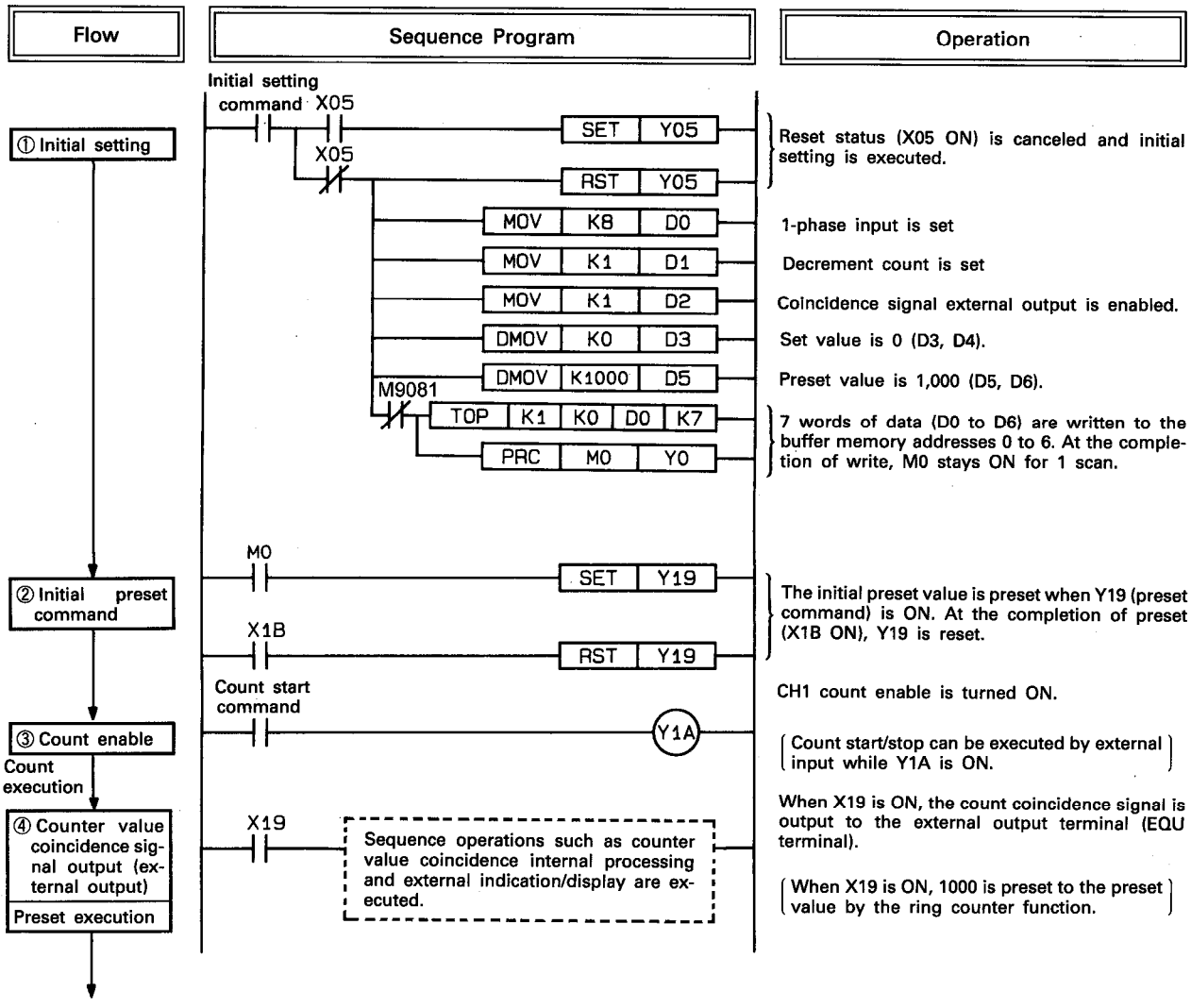

Flow
Sequence Program
Operation
④ Preset command (executed at the first/next count)
This part of the program is the same as from ④ count enable through ⑨ error code read/reset of Section 4.5.2.
⑤ Present value read after count end
Read to latch specified data register
Operation end
Preset command
M101
X1B
PLS M101
SET Y19
RST Y19
Execution of the first preset and execution of the second and subsequent presets.
Preset command (Y19) is turned OFF.
At the completion of preset (X1B ON), Y19 is turned OFF. X1B is turned OFF at the same time.
Present value read command
M9081
Given at count end
DFROP K1 K14 D100 K1
PRC M1 Y0
CH1 present value is read to the latch data register of D100, D101. Latch specifications vary according to parameter settings.
M1
Sequence operations such as PC power OFF OK indication (operation end) are executed.
Operation ends at the completion of reading of M1 ON.

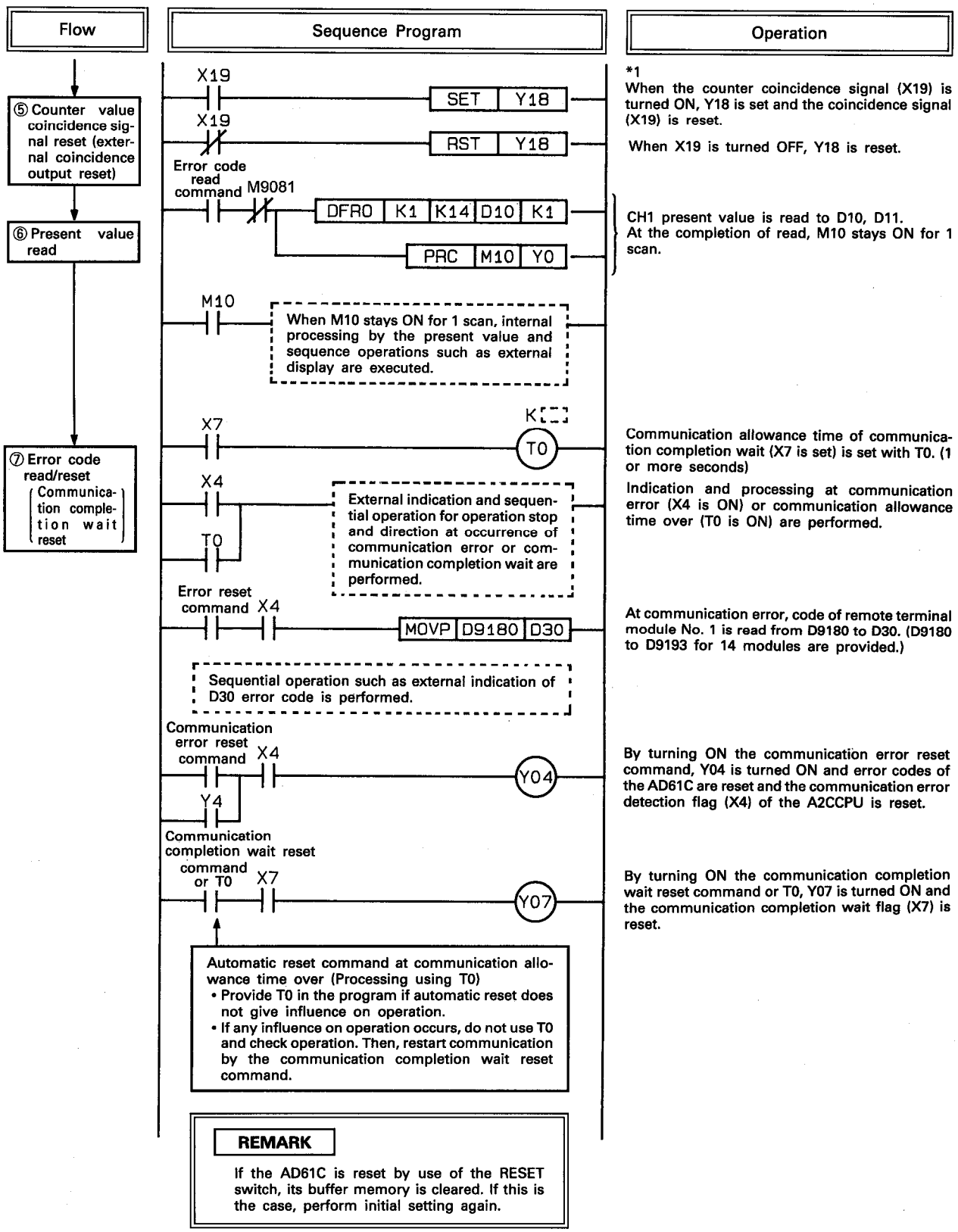
4.5.6 Example program of ring counter function

An example program in which ring count is executed by turning ON the ring counter switch is shown below.

This example program is explained according to the following conditions.

- The AD61C station number is set to 01 (occupying 1 to 4 stations)
- CH1 of the AD61C ring counter setting switch is turned ON.
- Only CH1 buffer memory is used and 1-phase is specified for the pulse input.
- Decrement count is specified.
- The external coincidence signal output is enabled.
- Preset is not executed by the external input.
- Count start/stop can be executed by the external input.
- The set value is 0 and the number of pulses for the preset value is 1000 (500 × 2).





*1: When using the ring counter function, be sure to reset the counter coincidence signal (X19). If X19 is left ON, the next preset cannot be executed.

4.5.7 Programs when 2 channels are used

Programs using 2 channels are explained.

(1) A CH2 example program is created in the same way as CH1 example programs in Sections 4.5.2 to 4.5.6.

(2) The execution content program of CH2 is added as indicated below following the order of the example program [Flow].

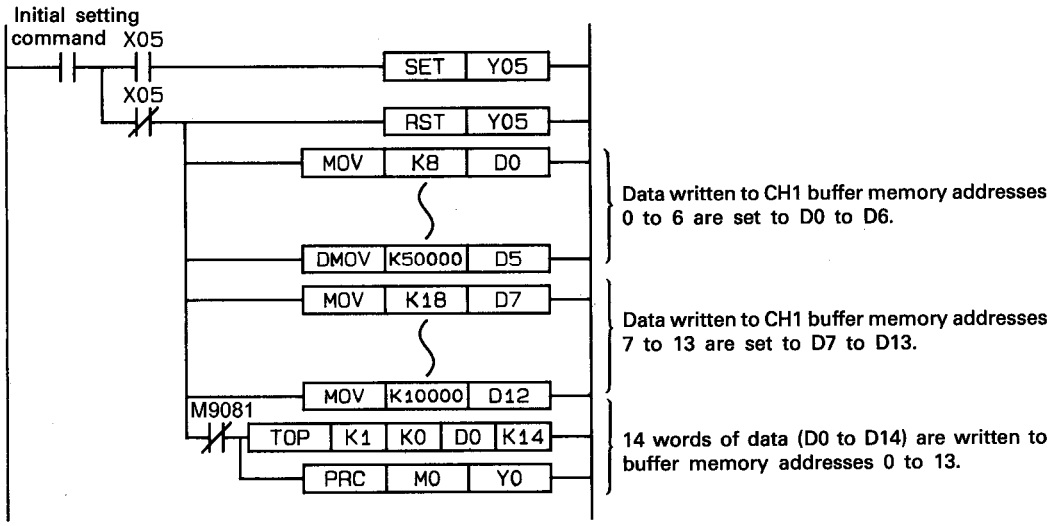
(3) Regarding FROM/TO instruction for the buffer memory, read/write is possible in batch in the range which the buffer memory addresses can be specified continuously.
(See [REMARK])

(4) FROM/TO instructions can be used for each buffer memory address.

(5) See Sections 4.3 and 4.4 regarding CH2 I/O signals and buffer memory addresses.

REMARK

• The program which writes CH1 and CH2 initial settings in batch is shown below.



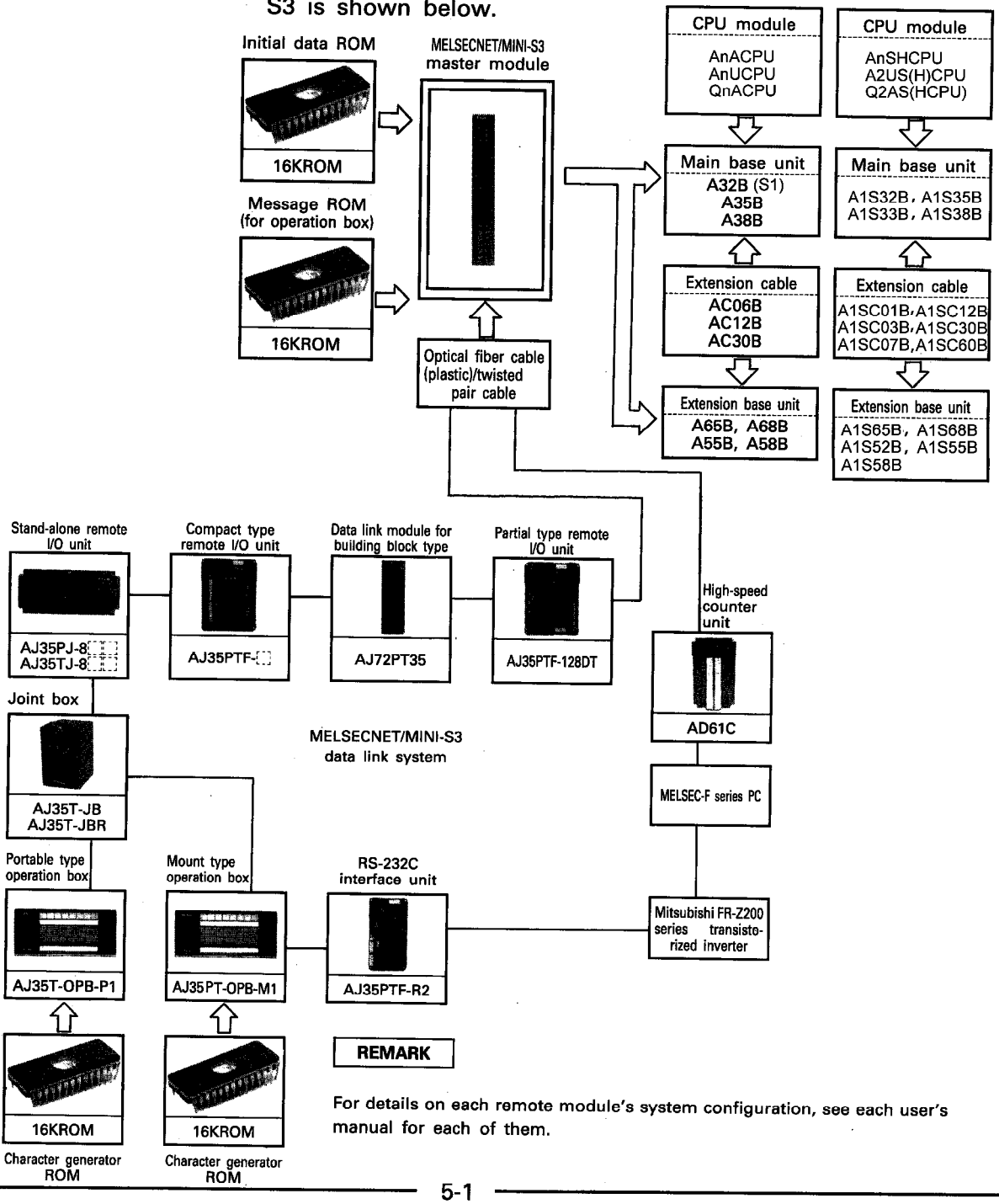
5. HOW TO LINK AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU AND MINI-S3 MASTER MODULE

- The AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU compatible GPP function software package is required to execute the link described in this chapter.
- When the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU compatible GPP function software package is not used, MELSECNET/MINI automatic refresh setting cannot be made. Therefore, follow the programming method described in Chapter 6, or correct only the I/O signal processing according to the program in Chapter 6.

5.1 System Configuration

5.1.1 Overall configuration

The overall configuration of the AD61C using MELSECNET/MINI-S3 is shown below.



REMARK

For details on each remote module's system configuration, see each user's manual for each of them.

5.1.2 Applicable system

The AD61C can be linked to the following CPUs via the MINI-S3 master module.

Applicable models	A1SHCPU A2SHCPU **A2ACPU (P21/R21)** **A2ACPU (P21/R21)-S1** **A3ACPU (P21/R21)** A2US(H)CPU	A2UCPU A2UCPU-S1 A3UCPU A4UCPU	Q2AS(H)CPU Q2AS(H)CPU-S1 Q2ACPU Q2ACPU-S1 Q3ACPU Q4ACPU

The MINI-S3 master module can be loaded into any slot and linked with the AD61C with the exception of (1) and (2) below. The number of device panels is unlimited.

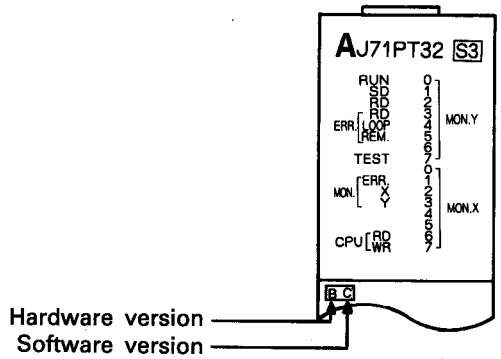
(1) If the AD61C is loaded into an extension base unit without a power supply module, the power capacity may be insufficient. Avoid loading as long as possible. If it is necessary to load, select power supply modules and extension cables with the power capacity of the main base unit's power supply module and extension cable voltage drops in mind. For details, see each CPU user's manual.

(2) In a MELSECNET data link system, loading is possible to both a master station and a local station.

(3) In a MELSECNET/10 network system, the AD61C can be loaded to either a control station or a normal station.
It is not applicable to a remote I/O station.

5.1.3 Cautions on constructing the system

(1) The software version shown below on the front of the AJ71PT32-S3 unit must be "C" or after to use the AD61C. The module of software version "A, B" or "no" software version indication cannot be used.



(2) When using the AD61C in the MELSECNET/MINI-S3 data link system, use twisted pair cables.

(3) Since each AD61C occupies 4 stations (a total of 32 I/O points), be careful when assigning I/O signals.

(4) When using the AD61C, set the MINI-S3 master module as follows.

a) Set the "jumper for mode selection" of the AJ71PT32-S3 to the extension mode (occupying 48 I/O points) of "48."

b) Create the initial data ROM for the MINI-S3 master module extension mode (occupying 48 I/O points) by the SW0GP-MINIP and install it. For remote terminal data setting at creation of the initial ROM, set the AD61C protocol to 4 : MINI STANDARD PROTOCOL.

c) For details, see each of the manuals below.
- AJ71PT32-S3 ,AJ71T32-S3,A1SJ71PT32-S3,A1SJ71T32-S3 type MELSECNET/MINI-S3 Master Module User's Manual
- SW0GP-MINIP Operating Manual

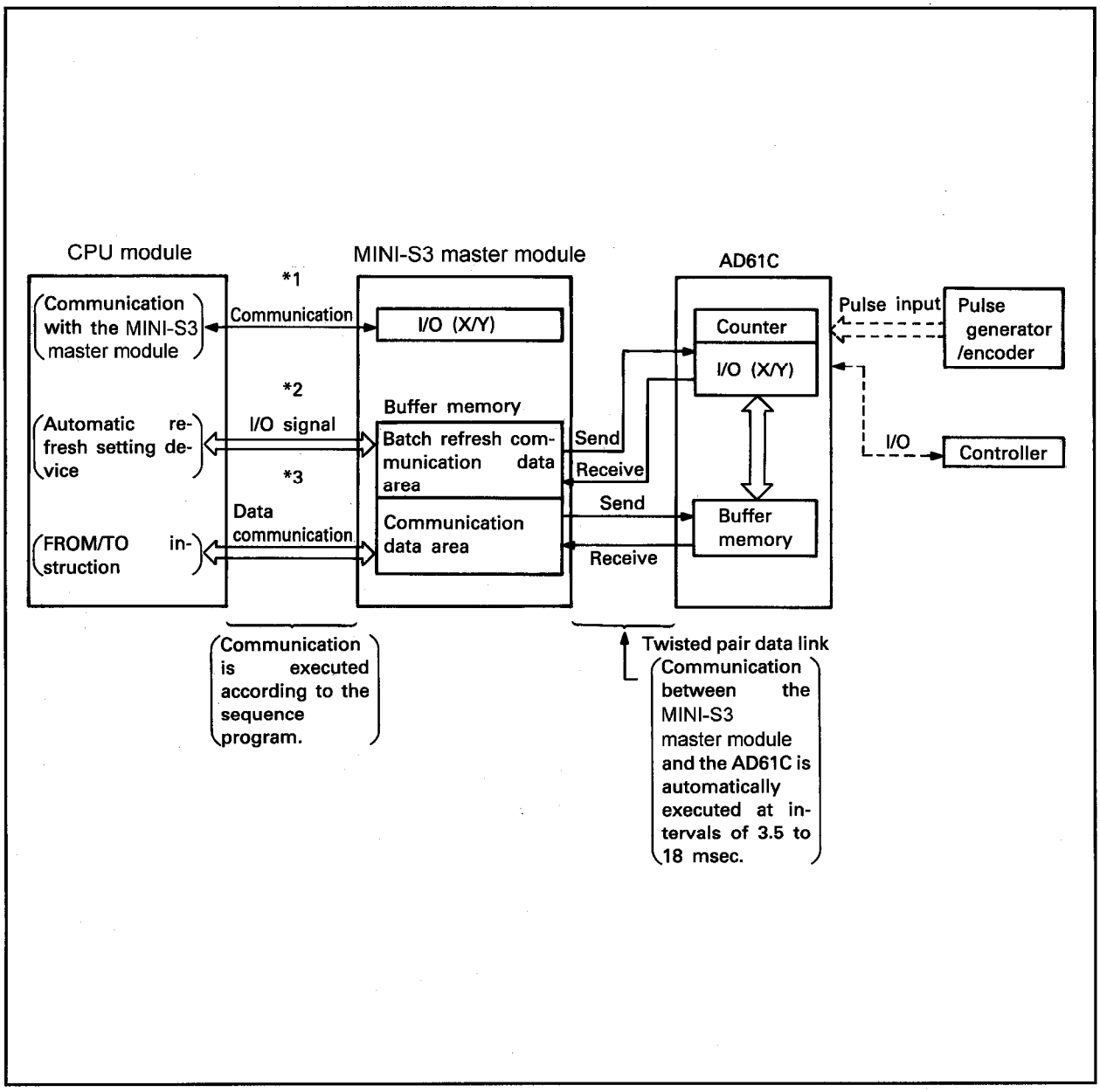
(5) The AD61C requires a 24 VDC power supply.
When supplying power from one power supply to multiple AD61Cs or to the link I/O modules, select cables and perform wiring taking voltage drops into consideration.

To calculate the receiving port voltage, see REMARK in Section 4.1.2.

5.2 Data Communication Processing

5.2.1 Communication method

(1) Communication between the AD61C and the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU is executed via the MINI-S3 master module' buffer memory. The communication method is shown below.



*1: I/O signal communication between the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU and the MINI-S3 master module is executed.
(I/O communication processing of communication start, error detection, etc.)

*2: Input signal communication between the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU and the MINI-S3 master module and between the MINI-S3 master module and the AD61C is executed. For details, see "I/O signal processing" in Section 5.2.2.

*3: Data communication between the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU and the MINI-S3 master module and between the MINI-S3 master module and the AD61C is executed.
For details, see "buffer memory data processing" in Section 5.2.3.

5.2.2 I/O signal processing

I/O signals (X,Y) of the AD61C to AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU are processed via the MINI-S3 master module buffer memory.

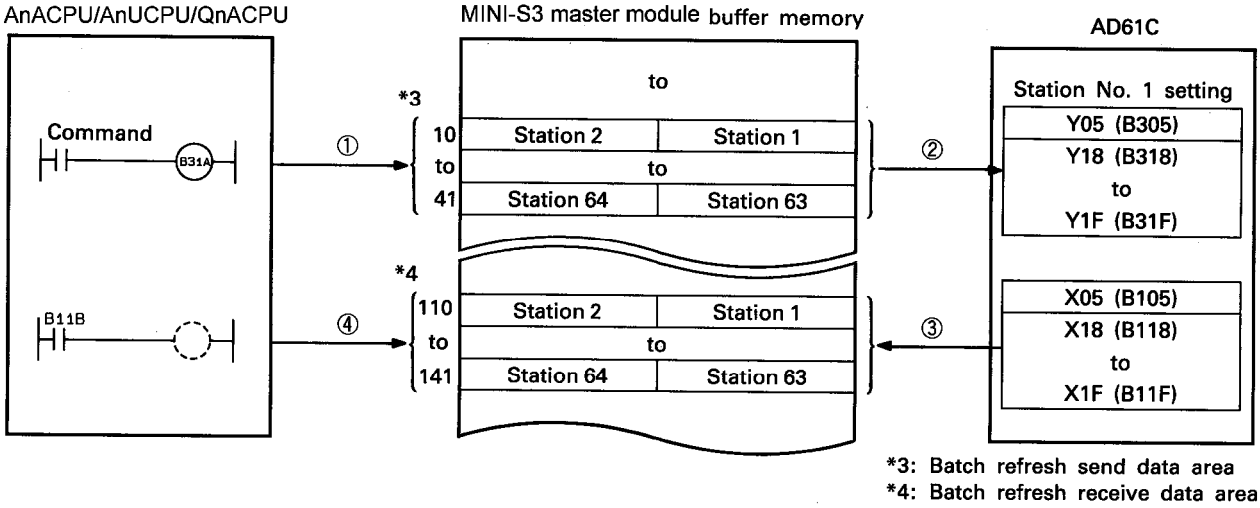
MELSECNET/MINI automatic refresh should be set by parameter settings and entered to the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU in advance.

By using the sequence program to turn ON/OFF the device numbers for which automatic refresh is set, AD61C I/O signals corresponding to the device number can be turned ON/OFF without acknowledging the MINI-S3 master module batch refresh send/ receive buffer memory.

(1) The I/O signal processing method between the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU and the AD61C is shown below.

- The AD61C station number is set to 01. (X00 to X1F, Y00 to Y1F)
- The automatic refresh communication device of AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU parameters is set to *1 B100 to B2FF (equivalent to input X) and *2 B300 to B4FF (equivalent to output Y).

*1: B100 to B2FF ····· 512 points (64 stations×8 points)
*2: B300 to B4FF ····· 512 points (64 stations×8 points)



*3: Batch refresh send data area
*4: Batch refresh receive data area

a) Output (Y) signal (communication order from ① to ②)

- By using the sequence program, the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU turns ON/OFF the device equivalent to the AD61C output (Y) assigned by the automatic refresh setting and writes it to the MINI-S3 master module batch refresh send data area.
- The MINI-S3 master module writes the send data to the AD61C output signal area.

b) Input (X) signal (communication order from ③ to ④)

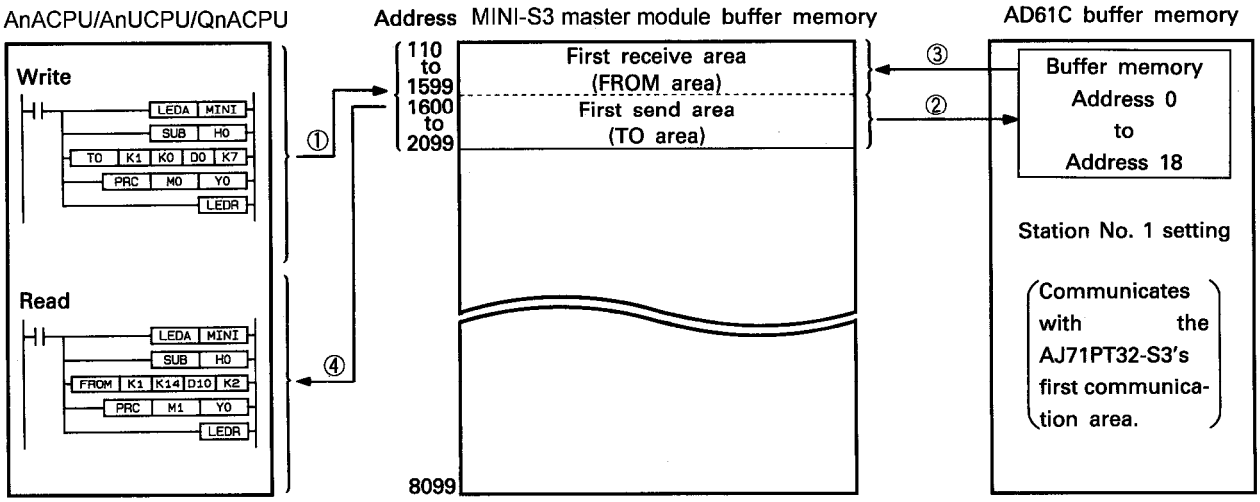
- The MINI-S3 master module always communicates with the AD61C and stores the AD61C input signal data in the batch refresh receive data area.
- Using the sequence program, the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU reads the ON/OFF data of the device equivalent to the AD61C input (X) assigned by the automatic refresh setting from the MINI-S3 master module batch refresh receive data area at every END processing, then turns the device ON/OFF.

5.2.3 Buffer memory data processing

The AD61C buffer memory data are processed via the MINI-S3 master module buffer memory. However, by using the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU dedicated read/write instructions, the AD61C buffer memory address can be specified directly to execute the TO/FROM instruction without acknowledging the MINI-S3 master module buffer memory address specification.

(1) The AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU AD61C buffer memory data processing method is shown below.

- The AD61C station number is set to 01.
- The MINI-S3 master module is loaded to slot 0. (head I/O No. ... H0)
- The AD61C is set to the first communication area of the remote terminal unit No. 1 by the MINI-S3 master module initial ROM.



a) Write to the AD61C buffer memory (communication order from ① to ②)

- By using the sequence program dedicated write instruction, the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU writes to the MINI-S3 master module send area. The MINI-S3 master module writes to the AD61C buffer memory.
- At the completion of write, the PRC instruction execution complete signal (M0) stays ON for 1 scan.

b) Read from the AD61C buffer memory (communication order from ③ to ④)

- By using the sequence program dedicated read instruction, read request is executed to the MINI-S3 master module.
- The MINI-S3 master module reads the data in AD61C buffer memory and stores it in the receive area.
- The AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU reads the receive data stored in the MINI-S3 master module.
- At the completion of read, the PRC instruction execution complete signal (M1) stays ON for 1 scan.

5.2.4 Processing time

The processing time required to write data to and read data from the AD61C buffer memory is shown below.

(1) Write processing time (T_W)

T_W = {(number of data written) + 8} × t + 10 + (ACPU scan time) [ms]

(2) Read processing time (T_R)

T_R = {(number of data read) + 9} × t + 10 + (ACPU scan time) [ms]

(3) "t" is the I/O refresh time.
It varies according to the number and type of connected remote module stations.
Calculation of the I/O refresh time is shown below.

Mode	Operation Mode Setting	I/O Refresh Time (ms)
Extension mode	Automatic return enable (0)	t=0.66+(0.044×R)+(0.25×B)+(0.95×T)
	Automatic return disable (1)	t=0.54+(0.058×R)+(0.25×B)+(0.95×T)
	Communication stop at error detection (2)	t=0.54+(0.051×R)+(0.25×B)+(0.95×T)

R: Total number of remote stations
B: Number of AJ35PTF-128DTs
T: Number of remote terminal units

POINT

(1) Count start/stop by external input, preset, and the counter coincidence signal by external output respond in less than 10 msec.
(2) To increase the processing time responsiveness of sequence operations, use external I/O signals.

REMARK

1) *1: Number of system data communications between master module and AD61C
2) *2: A61C internal processing time

5.3 I/O Signals to/from PLC CPU

5.3.1 AD61C I/O signals

I/O signals when the AD61C station No. is 01 (X/Y00 to X/Y1F) are shown below.

(1) Input signals (Signal direction: AD61C → PLC CPU)

Device No.		Signal	Operation Status
CH1	CH2		
X00 to X04		(Unused)	—
X05		Reset status detection	• Latched upon AD61C power application or when reset switch is ON. • When reset status detection reset (Y05) is turned ON, X05 turns OFF.
X06 to X17		(Unused)	—
X18	X1C	CH1/CH2 counter value comparison	• ON: Counter value≧set value. • OFF: Counter value<set value.
X19	X1D	CH1/CH2 counter value coincidence	• Latched if counter value=set value. • When the coincidence signal reset command (Y18, Y1C) is turned ON, X19 and X1D turn OFF.
X1A	X1E	CH1/CH2 external preset request detection	• Latched if an external preset request is given. • When the external preset request detection reset (Y1B, Y1F) is turned ON, X1A and X1E turn OFF.
X1B	X1F	CH1/CH2 preset completion	• Latched at the completion of preset when the preset command (Y19, Y1D) is ON. • When the preset command (Y19, Y1D) is turned OFF, X1F turns OFF.

(2) Output signals (Signal direction: PLC CPU → AD61C)

Device No. CH1	Device No. CH2	Signal	Operation Status
Y00 to Y04		(Unused)	—
Y05		Reset of reset status detection	• When reset status detection reset (Y05) is turned ON, preset status detection (X05) turns OFF. • When X05 is OFF, Y05 turns OFF.
Y06 to Y17		(Unused)	—
Y18	Y1C	CH1/CH2 coincidence signal reset command	• If the coincidence signal reset command (Y18, Y1C) is turned ON, the counter coincidence signal (X19, X1D) and the external output (EQU) turn OFF. • When X19 and X1D are OFF, Y18 and Y1C turn OFF.
Y19	Y1D	CH1/CH2 preset command	• At the rising edge from OFF to ON (⌐) of the preset command (Y19, Y1D), the preset value is written. • At the completion of preset (X1B, X1F), Y19 and Y1D turn OFF.
Y1A	Y1E	CH1/CH2 count enable	• When count enable (Y1A, Y1E) is turned ON, counting is enabled. • When count enable (Y1A, Y1E) is turned OFF, counting is disabled.
Y1B	Y1F	CH1/CH2 external preset request detection reset	• When external preset request detection reset (Y1B, Y1F) is turned ON, external preset request detection (X1A, X1E) turns OFF. • When X1A and X1E are OFF, Y1B and Y1F turn OFF.

5.3.2 MINI-S3 master module I/O signals

I/O signals between the MINI-S3 master module and the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU in the extension mode are used when accessing the AD61C buffer memory.
For details about the I/O signals, see the MELSECNET/MINI-S3 Master Module User's Manual.
The list of I/O signals in the extension mode is shown below. "n" in the Device No. column of the table is the master module head I/O number. It is determined by the number of I/O points of the I/O modules loaded into the master module's front slot and by the master module's position.

Example: When the master unit head I/O number is "X/Y20"
X (n+0) to X (n+2F)=X20 to X4F
Y (n+0) to Y (n+2F)=Y20 to Y4F

Device No.	Signal		Device No.	Signal	
X (n+0)	Send complete signal	For remote terminal unit No. 1	Y (n+0)	Send complete signal	For remote terminal unit No. 1
X (n+1)	Read request signal		Y (n+1)	Read request signal	
X (n+2)	Send complete signal	For remote terminal unit No. 2	Y (n+2)	Send complete signal	For remote terminal unit No. 2
X (n+3)	Read request signal		Y (n+3)	Read request signal	
X (n+4)	Send complete signal	For remote terminal unit No. 3	Y (n+4)	Send complete signal	For remote terminal unit No. 3
X (n+5)	Read request signal		Y (n+5)	Read request signal	
X (n+6)	Send complete signal	For remote terminal unit No. 4	Y (n+6)	Send complete signal	For remote terminal unit No. 4
X (n+7)	Read request signal		Y (n+7)	Read request signal	
X (n+8)	Send complete signal	For remote terminal unit No. 5	Y (n+8)	Send complete signal	For remote terminal unit No. 5
X (n+9)	Read request signal		Y (n+9)	Read request signal	
X (n+A)	Send complete signal	For remote terminal unit No. 6	Y (n+A)	Send complete signal	For remote terminal unit No. 6
X (n+B)	Read request signal		Y (n+B)	Read request signal	
X (n+C)	Send complete signal	For remote terminal unit No. 7	Y (n+C)	Send complete signal	For remote terminal unit No. 7
X (n+D)	Read request signal		Y (n+D)	Read request signal	
X (n+E)	Send complete signal	For remote terminal unit No. 8	Y (n+E)	Send complete signal	For remote terminal unit No. 8
X (n+F)	Read request signal		Y (n+F)	Read request signal	
X (n+10)	Send complete signal	For remote terminal unit No. 9	Y (n+10)	Send complete signal	For remote terminal unit No. 9
X (n+11)	Read request signal		Y (n+11)	Read request signal	
X (n+12)	Send complete signal	For remote terminal unit No. 10	Y (n+12)	Send complete signal	For remote terminal unit No. 10
X (n+13)	Read request signal		Y (n+13)	Read request signal	
X (n+14)	Send complete signal	For remote terminal unit No. 11	Y (n+14)	Send complete signal	For remote terminal unit No. 11
X (n+15)	Read request signal		Y (n+15)	Read request signal	
X (n+16)	Send complete signal	For remote terminal unit No. 12	Y (n+16)	Send complete signal	For remote terminal unit No. 12
X (n+17)	Read request signal		Y (n+17)	Read request signal	
X (n+18)	Send complete signal	For remote terminal unit No. 13	Y (n+18)	Send complete signal	For remote terminal unit No. 13
X (n+19)	Read request signal		Y (n+19)	Read request signal	
X (n+1A)	Send complete signal	For remote terminal unit No. 14	Y (n+1A)	Send complete signal	For remote terminal unit No. 14
X (n+1B)	Read request signal		Y (n+1B)	Read request signal	
X (n+1C)	(Unused)		Y (n+1C)	(Unused)	
X (n+1D)			Y (n+1D)		
X (n+1E)			Y (n+1E)		
X (n+1F)			Y (n+1F)		
X (n+20)	Hardware error		Y (n+20)		
X (n+21)	MINI-S3 link communication in progress		Y (n+21)		
X (n+22)	(Unused)		Y (n+22)		
X (n+23)	Receive data clear complete (for the AJ35PTF-R2)		Y (n+23)	Receive data clear request (for the AJ35PTF-R2)	
X (n+24)	Remote terminal unit error detection		Y (n+24)	Remote terminal unit error detection reset	
X (n+25)	Test mode		Y (n+25)	(Unused)	
X (n+26)	MINI-S3 link error detection		Y (n+26)		
X (n+27)	MINI-S3 link communication error		Y (n+27)		
X (n+28)	ROM error		Y (n+28)	MINI-S3 link communication start	
X (n+29)	(Unused)		Y (n+29)	(Unused)	
X (n+2A)			Y (n+2A)	FROM/TO instruction response specification	
X (n+2B)			Y (n+2B)	Error station data clear specification	
X (n+2C)			Y (n+2C)	Buffer memory channel switching	
X (n+2D)			Y (n+2D)	Error reset	
X (n+2E)			Y (n+2E)	(Unused)	
X (n+2F)			Y (n+2F)		

I/O signal List in the Extension Mode

5.4 Buffer Memory Assignment

5.4.1 AD61C buffer memory

The AD61C does not have battery backup. When power is turned OFF or when the AD61C is reset, the buffer memory will be cleared (initialized).
When the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU is reset, the coincidence signal output enable flag of CH1, CH2 (CH1=2, CH2=9) will be initialized.
Memory buffer assignment is shown below.

Address (decimal)	Name	Description	Read/Write (FROM/TO)	Initial Value
0	CH1 mode register	• 1 or 2-phase input specification • See (1) for data to be specified.	TO (FROM)	18
1	CH1 operation count specification	• Increment/decrement specification • See (2) for data to be specified.	TO	0
2	CH1 coincidence signal output enable flag	• Specification when coincidence signal is output to outside • See (3) for data to be specified.	TO	0
3	CH1 set value	• Storage of higher and middle digit data of set value	TO (FROM)	
4		• Storage of lower digit data of set value		
5	CH1 preset value	• Storage of higher and middle digit data of preset value	TO	0
6		• Storage of lower digit data of preset value		
7	CH2 mode register	• 1 or 2-phase input specification • See (1) for data specified.	TO (FROM)	18
8	CH2 operation count specification	• Increment/decrement specification • See (2) for data specified.	TO	0
9	CH2 coincidence signal output enable flag	• Specification when coincidence signal is output to outside • See (3) for data to be specified.	TO	0
10	CH2 set value	• Storage of higher and middle digit data of set value	TO (FROM)	
11		• Storage of lower digit data of set value		
12	CH2 preset value	• Storage of higher and middle digit data of preset value	TO	0
13		• Storage of lower digit data of preset value		
14	CH1 present value	• Storage of higher and middle digit data of present value	FROM	
15		• Storage of lower digit data of present value		
16	CH2 present value	• Storage of higher and middle digit data of present value		
17		• Storage of lower digit data of present value		
18	Error code	• Storage of the error code of the first error		

(1) Mode register's written data (CH1=0, CH2=7)

	Written Data	Initial Value
Used by 1-phase	8	18 (2-phase)
Used by 2-phase	18	

(Caution)
If data other than 8, 18 are written, an error occurs. The error code will be set to address 18 and counting controlled by the initial value.

(2) Decrement count command's written data (CH1=1, CH2=8)
Valid only for 1-phase inputs.

	Written Data	Initial Value
Decrement count specification	1	0 (Increment)
Increment count specification	0	

(Caution)
Data written are valid only for the lower 1 bit. The upper 15 bits will be ignored.

(3) Coincidence signal output enable flag's written data (CH1=2, CH2=9)

	Written Data	Initial Value
Enable	1	0 (disabled)
Disable	0	

(Caution)
Written data are valid only for the lower 1 bit. The upper 15 bits will be ignored.

POINT

Since increment/decrement count of phases A and B of a 2-phase input will automatically be determined, the contents of the buffer memory will be invalid.

5.4.2 MINI-S3 master module buffer memory

There are communication (send/receive) data addresses for the MINI-S3 master module buffer memory according to dedicated read/write instructions between the MINI-S3 master module and the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU.
The assignment of buffer memory addresses which automatically communicate with the AD61C is shown below.
For details of the buffer memory, see the MELSECNET/MINI-S3 Master Module User's Manual.

	Address (decimal)		Content	PC CPU Read/write Enable/disable
	0	Total number of remote stations	The range of the station numbers of all connected remote units is set.	Read/write enable
	1	Number of retries	The number of retries at communication error occurrence is set.	
		(Unused)	—	
	4	Line error check	Used to confirm line faulty areas.	
		(Unused)	—	
*1	10 to 41	Batch refresh send data	Data output to the batch refresh type remote I/O module are written.	
		(Unused)	—	—
	70 to 77	Remote unit's card data	Each connected remote unit's type is stored.	Read only
		(Unused)	—	—
	90 to 93	Accumulation faulty station detection	Station numbers of remote units which are in communication error are stored. (Detection status is retained until reset.)	Read/write enable
		(Unused)	—	—
	100 to 103	Faulty station detection	Station number of remote unit which is in communication error is stored. (Communication status is always updated.)	Read only
		(Unused)	—	
	107	Communication error code	The cause of the MINI-S3 link communication error signal being ON is stored.	
	108	Error detection code	The accumulated number of times the MINI-S3 link error detection turns ON is stored.	
		(Unused)	—	
*2	110 to 141	Batch refresh receive data	Input data from batch refresh type remote I/O module are stored.	
		(Unused)	—	
	160	Line error retry counter	The number of executions of retry processing when communication with all remote units is disabled by line error is stored.	
	161 to 192	Retry counter	The number of times retry processing to faulty stations is executed is stored.	
		(Unused)	—	
*3	195	Remote terminal unit faulty stations	The station number of the remote terminal unit with which an error has occurred is stored.	
	196 to 209	Remote terminal unit error code	The cause of the remote terminal unit error detection signal [X (n+24)] being ON is stored.	
		(Unused)	—	—
	250 to 282	Partial refresh station	Partial refresh type remote I/O module station No. and specification of the number of digits are written.	Read/write enable
		(Unused)	—	
	300 to 363	Partial refresh send data	Data output to the partial refresh type remote I/O module are written.	
		(Unused)	—	
	598	Partial refresh accumulation input error detection	Partial refresh type remote I/O module's input data received faulty station is stored. (Detection status is retained until reset.)	
	599	Partial refresh input error detection	Partial refresh type remote I/O module's input data received faulty station is stored. (Communication status is always undated.)	
	600 to 663	Partial refresh receive data	Partial refresh type remote I/O module's input data are stored.	Read only

*1: Output signal data write area to the AD61C
*2: Store area of the input signal data from the AD61C
*3: Area which stores station number and error code when an AD61C error occurs. (See Section 8.1 for error codes.)

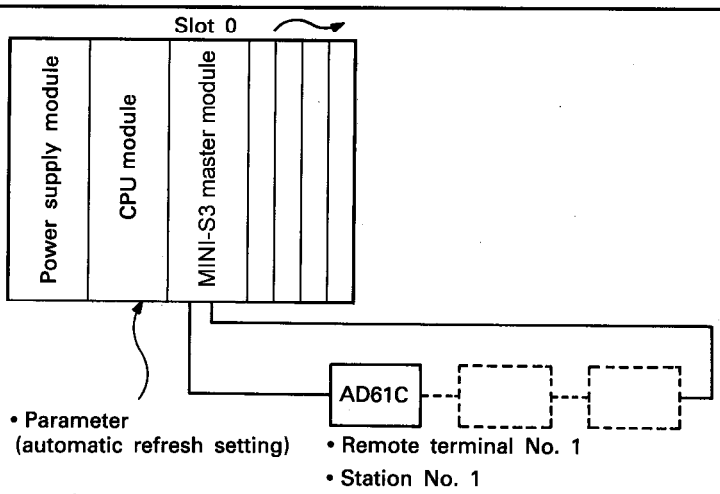
Address (decimal)		Content	PC CPU Read/write Enable/disable
*4 858	Receive data clear specification	The AJ35PTF-R2 station number which executes receive data clear by the receive data clear request signal [Y (n+23)] is specified.	Read/write enable
*4 859	Receive data clear range specification	The receive buffer which is cleared when the receive data clear is executed by the receive data clear request signal [Y (n+23)] is specified.	
860 to 929	No-protocol mode parameter	Parameters when using the AJ35PTF-R2 in a no-protocol mode are set.	
930 to 1099	(Unused)	—	—

Address (decimal)	CH0	CH1	Content	PC CPU Read/write Enable/disable
*5 1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8	Send data to the remote terminal unit write area, or, receive data from the remote terminal unit store area.	Read/write enable
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9		
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10		
4100 to 5099	Communication area for remote terminal No. 4	Communication area for remote terminal No. 11		
5100 to 6099	Communication area for remote terminal No. 5	Communication area for remote terminal No. 12		
6100 to 7099	Communication area for remote terminal No. 6	Communication area for remote terminal No. 13		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14		
	[Y (n+2C) at OFF]	[Y (n+2C) at ON]		

*4: Clear processing area of receive data by the AD61C reset operation
*5: Buffer memory area for AD61C data transfer (1st module to 14th module)

5.5 Programming

Programming is explained below under the following setting conditions of AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU, MINI-S3 master module, and AD61C.

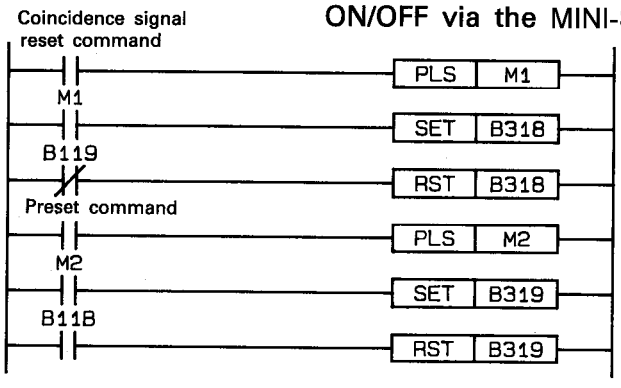


1) Input signal assignment (assigned to link relay B) of the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU parameter automatic refresh setting
   - Batch refresh receive data
     ..... B100 to B2FF (For X00 to X1F of AD61C)
   - Batch refresh send data
     ..... B300 to B4FF (For Y00 to Y1F of AD61C)
2) MINI-S3 master module is loaded to slot 0 (occupying 48 points: I/O No. X/Y00 to X/Y2F)
3) AD61C remote terminal number is set to "1" (initial ROM)
4) AD61C station number is set to "01" (occupying stations Nos. 1 to 4)

5.5.1 Basic programs

Basic programs to control the AD61C via the MINI-S3 master module are explained below.

(1) I/O signal processing program (X18 to X1F, Y18 to Y1F)
   a) Link relay "B" assigned by the parameter automatic refresh setting is used.
   b) The AD61C I/O signal (X/Y) equivalent to "B" is turned ON/OFF via the MINI-S3 master module.



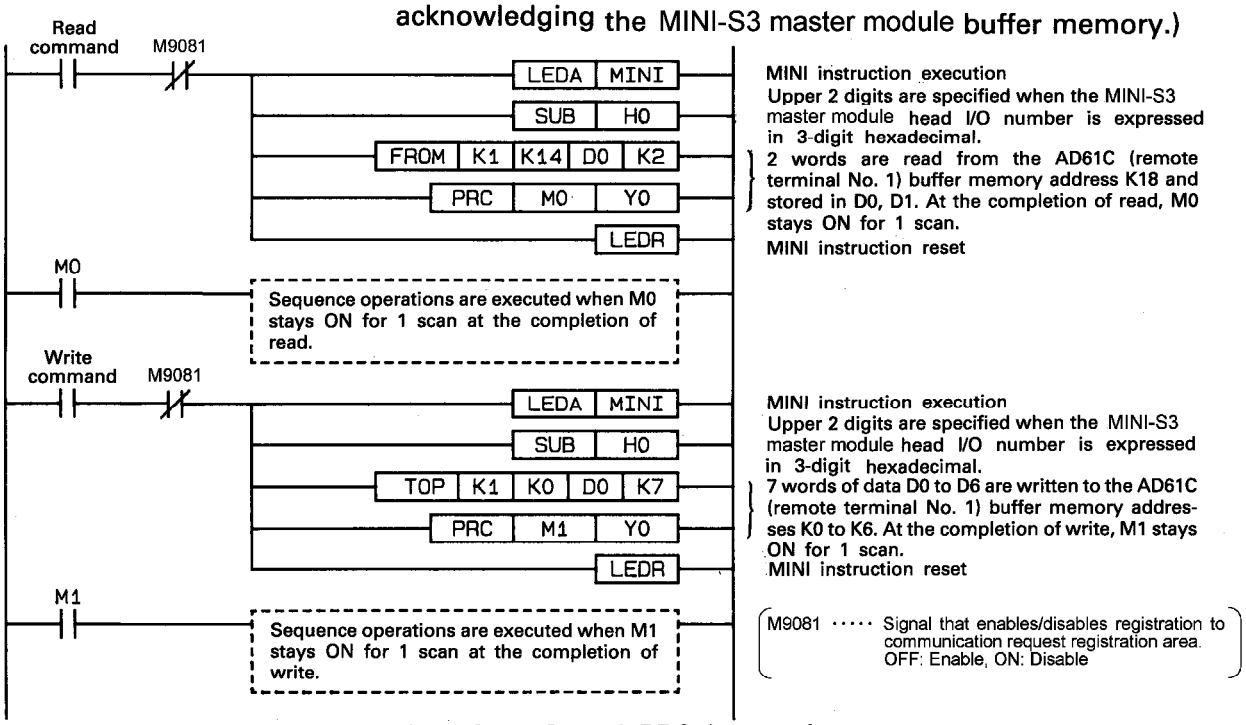
B318 (equivalent to the AD61C's Y18) is set.

B318 (Y18) is reset when B119 (equivalent to the AD61C's X19) is turned OFF.

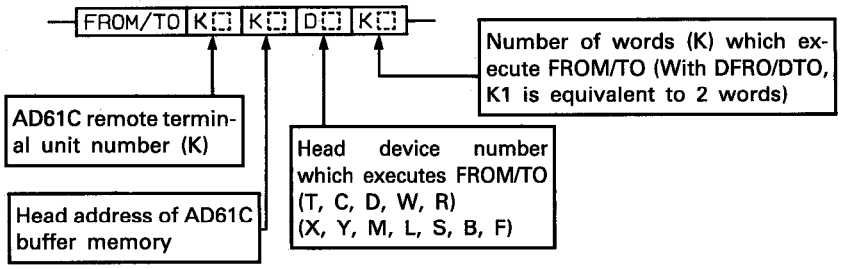
B319 (equivalent to the AD61C's Y19) is set.

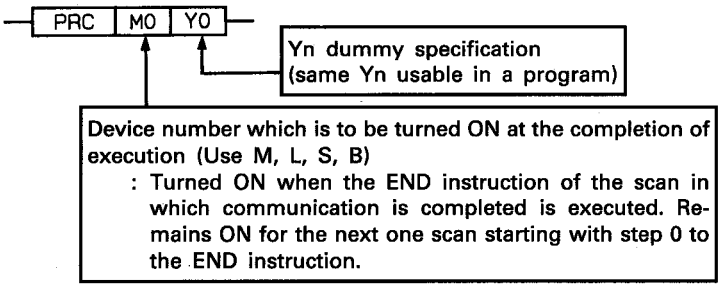
B319 (Y19) is reset when B11B (equivalent to the AD61C's X1B) is turned ON.

(2) Buffer memory processing program
Read/write of buffer memory is executed by directly designating AD61C buffer memory addresses using AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU dedicated instructions via the MINI-S3 master module. (The AD61C buffer memory can be used without acknowledging the MINI-S3 master module buffer memory.)



a) FROM/TO and PRC instructions
For details about FROM/TO and the PRC instruction, see the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU programming manual.

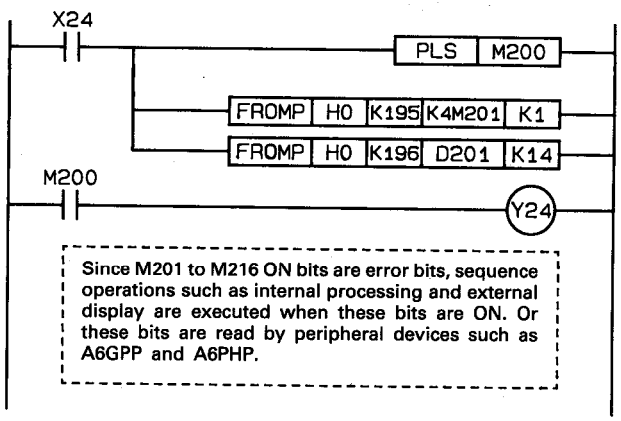




POINT

When the FROM/TO instruction is executed by the sequence program, data communication is executed via the MINI-S3 master module buffer memory. When the execution completion device of the PRC instruction is turned ON, data communication ends.

(3) Error detection program
MINI-S3 master module buffer memory K195 (remote terminal unit faulty station) and K196 to K209 (remote terminal unit error code) are read.



Buffer memory is read when X24 (error detection) is ON and reset command is executed.

Faulty station read (Faulty stations: M201 to M216 when bit ON)
The error codes of terminals No. 1 to No. 14 are read to D201 to D214.

When M200 is ON, Y24 turns ON and X24 turns OFF.

After staying ON for 1 scan, Y24 turns OFF.

a) The error code which is detected by MINI-S3 master module is shown below.

Error Code (decimal)	Error Name	Error Content	Corrective Action
1	Set data error	There is an error in the data set to the AD61C send area.	Set correct data.
6	WDT error	AD61C is malfunctioning.	Confirm the AD61C LED indicators and correct following AD61C troubleshooting procedure.
8	Send area set error	AD61C send area size is insufficient.	Set the send area of the required number of bytes as send data to the AD61C.
9	Communication error	Normal communication between the master module and the AD61C cannot be executed.	• Noise ····· Execute communication again. • Check the AD61C for possible hardware error.
11			
10	Receive area set error	AD61C receive area size is insufficient.	Set the receive area of the required number of bytes as receive data from the AD61C.

b) In addition to the above error code, the error code which the AD61C detects is sent to the MINI-S3 master module and is stored in the MINI-S3 master module buffer memory. (For the AD61C error code, see Section 8.1.)

(4) Data clear processing program by AD61C reset operations and allowable communication time over

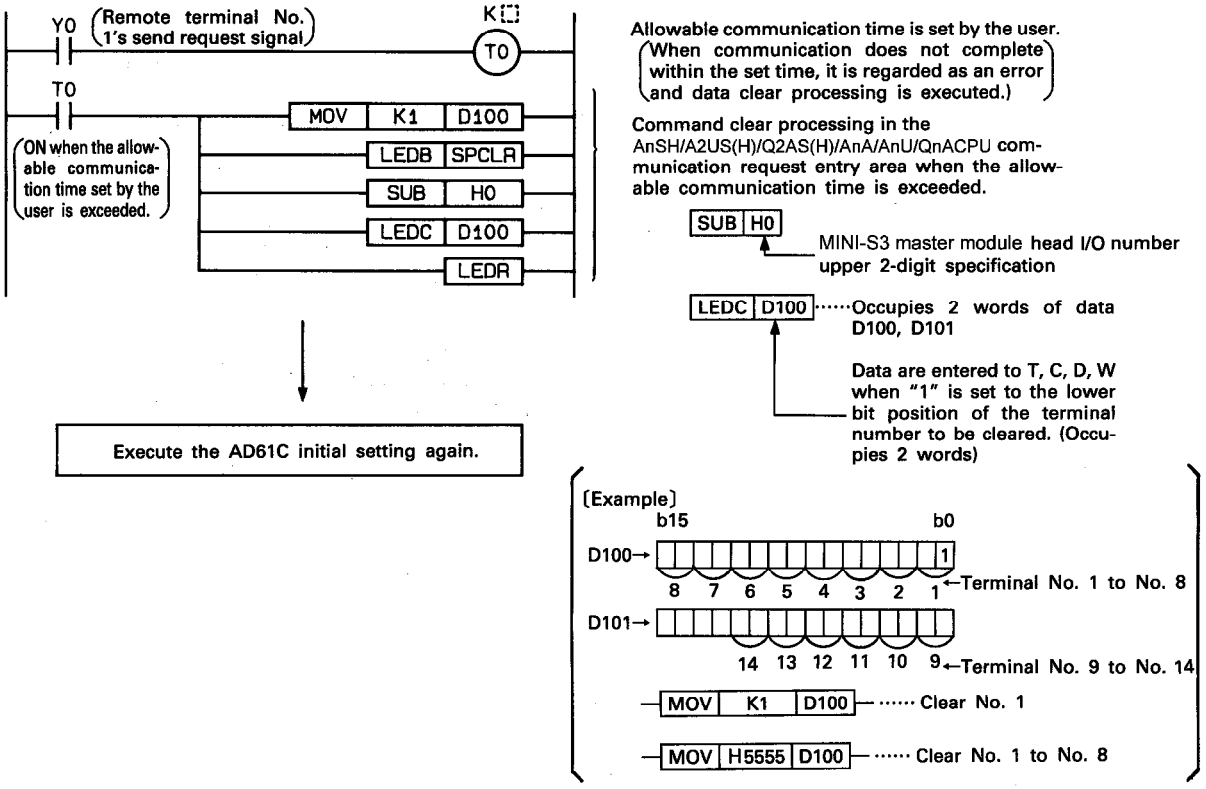
a) When the AD61C's front reset switch is operated during communication, it is necessary to write the initial data again after detecting the reset operation and clearing the MINI-S3 master module receive data by the sequence program.

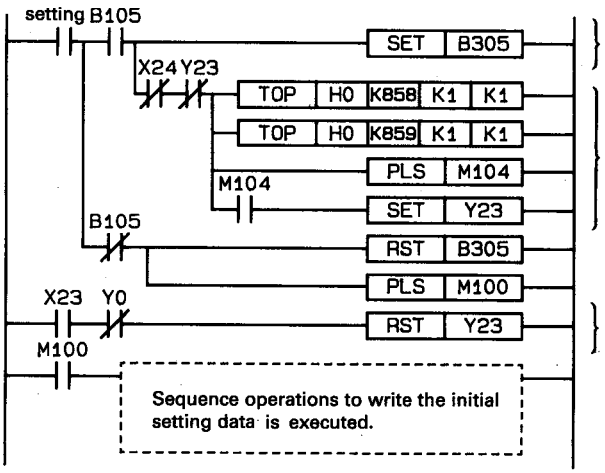
- If initial setting is not executed again after reset operations, the AD61C will not operate correctly.
- Create a sequence program which clears command data in the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU communication request entry area during initial setting under the conditions that both reset status detection and reset status detection reset are ON.

b) When the reset switch is pressed and a non-sending status to the AD61C has occurred, such status will remain. Therefore, set the allowable communication time by the timer, execute data clear, and re-execute the send request.

c) For the detection of the AD61C reset status, create a program using parameter automatic refresh setting link relay "B" equivalent to AD61C I/O signals.

- Reset status detection ····· X05 ON → B105 ON
- Reset status detection is reset ···· Y05 ON → B305 ON
  [When B305 (Y05) is ON, B105 (X05) turns OFF.]





The reset status detection is reset and command data in the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU communication request entry area are cleared.

With B105 (X05) ON by reset operations, MINI-S3 master module receive data clear processing ("1" written to the buffer memory) is executed.
(The master module is cleared so that communication can be executed again. However, the contents of the receive data area will not be cleared.)

At the completion of clear (X23 ON), the clear request (Y23) turns OFF and at the same time X23 turns OFF.

5.5.2 Example 1-phase/2-phase input counting programs

(1) Example counting programs for 1-phase/2-phase inputs are explained below.
- The settings for the AD61C, MINI-S3 master module , and AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU are as described in Section 5.5. (I/O signals are assigned to B100 to B4FF by parameter automatic refresh setting.)
- CH1 is used.
- 1-phase is specified for the pulse input. (The 2-phase setting is entered in the "operation" column below.)
- Decrement count is set.
- The external coincidence signal's output is enabled.
- Preset is not executed by the external input. (Count start/ stop can be executed by the external input.)
- The counter present value is not preset.
- The ring counter function is not used.

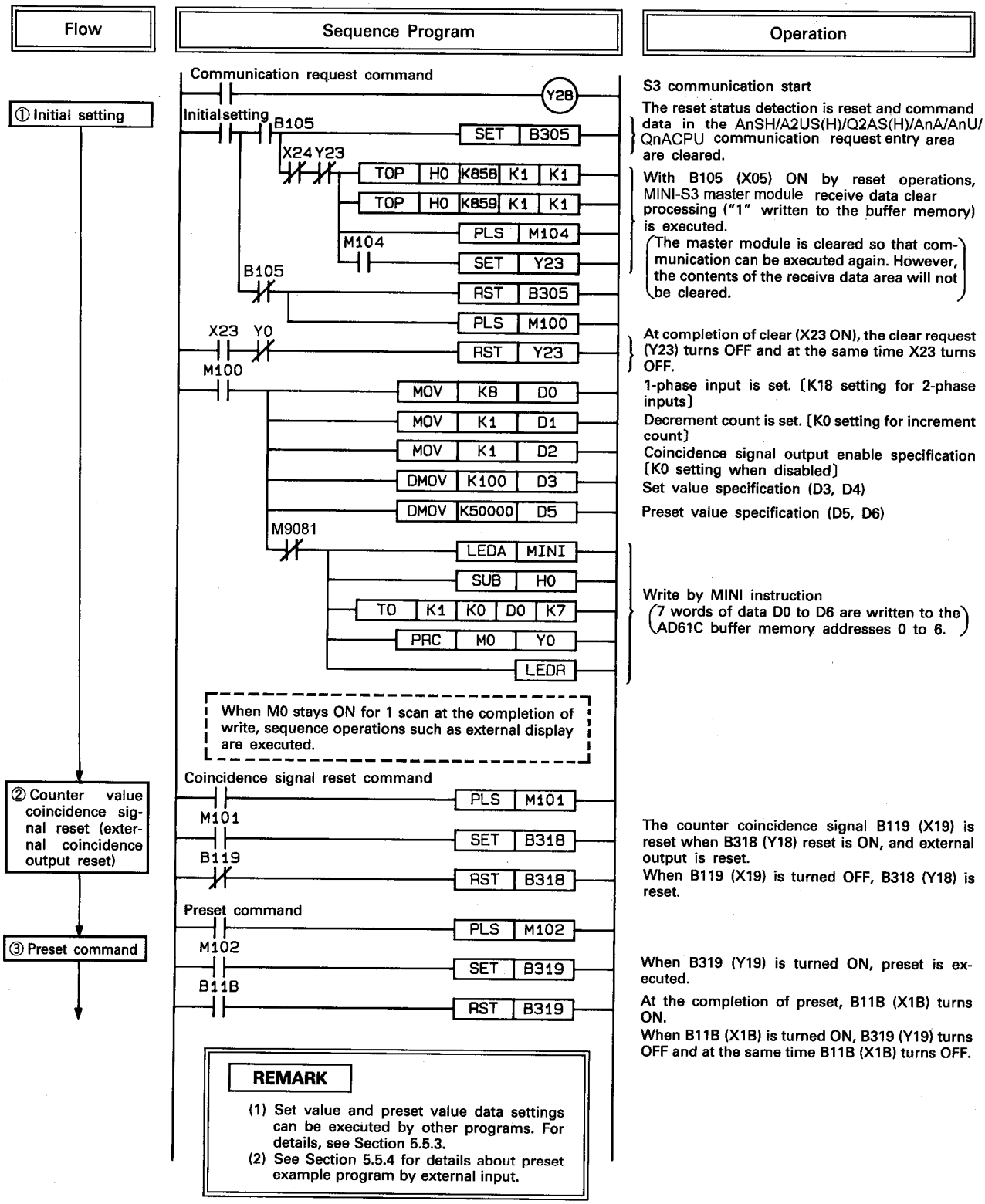
(2) The following example program is explained: initial setting, coincidence signal reset, preset, count start, coincidence processing, present value read, error detection/error code read, error code reset, data clear processing by reset operations.

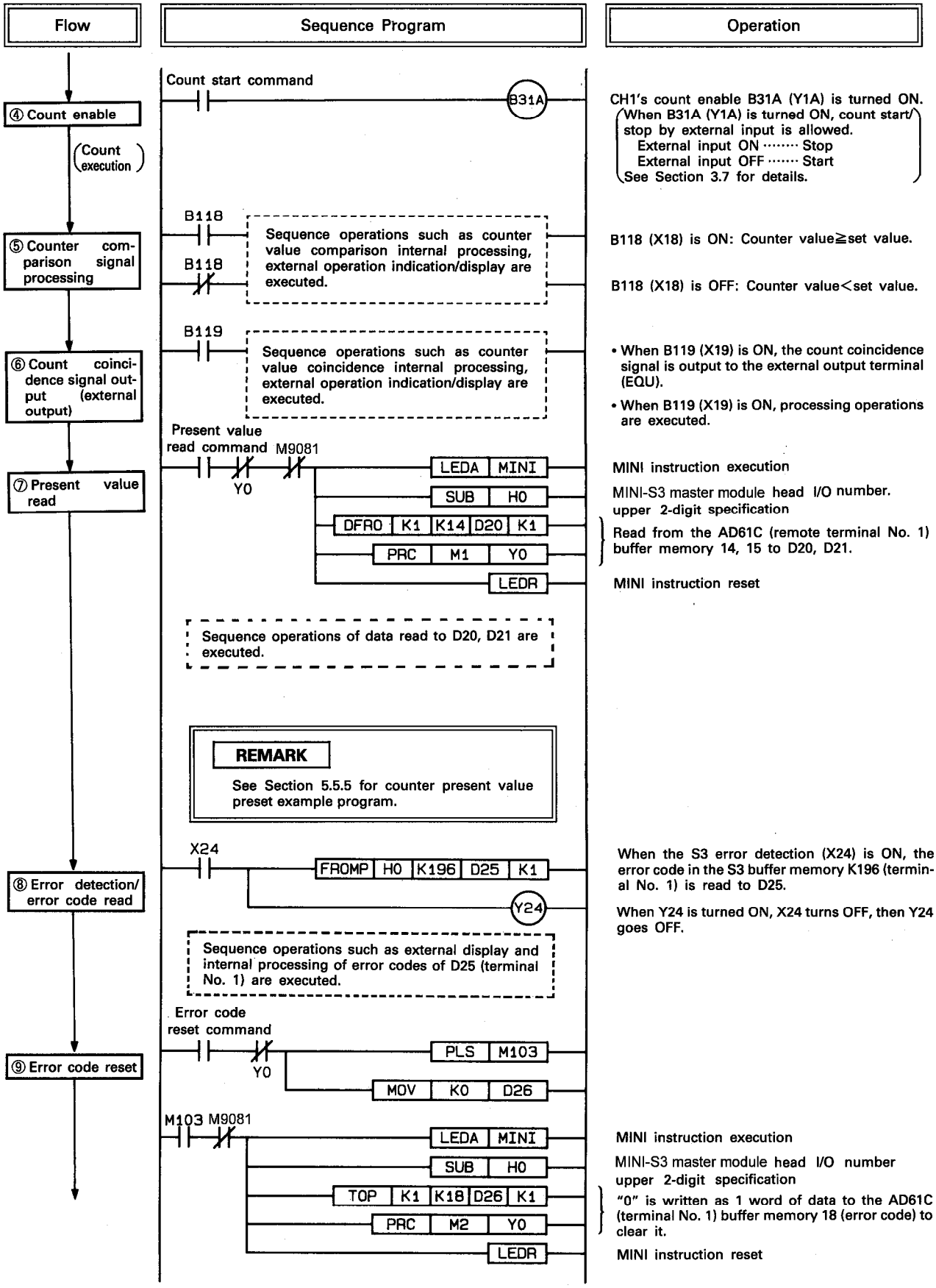
(3) The operation items of the program order are explained in the "flow" column.

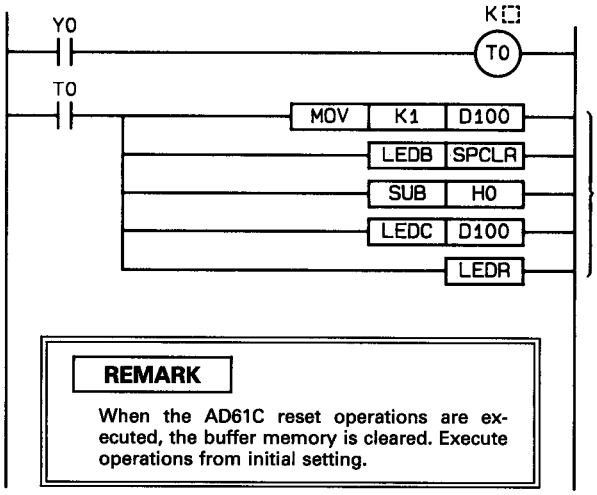
(4) The example program is explained in the "Operation" column.

(5) Initial setting values of the example program are written to the AD61C's buffer memory in batch.

(6) Since the AD61C goes to the initial state when the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU is reset or the AD61C's reset switch is turned ON, execute initial setting again.


Flow
Sequence Program
Operation
① Initial setting
② Counter value coincidence signal reset (external coincidence output reset)
③ Preset command
Communication request command
Y28
S3 communication start
Initial setting
B105
SET B305
The reset status detection is reset and command data in the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU communication request entry area are cleared.
X24 Y23
TOP H0 K858 K1 K1
TOP H0 K859 K1 K1
PLS M104
M104
SET Y23
With B105 (X05) ON by reset operations, MINI-S3 master module receive data clear processing ("1" written to the buffer memory) is executed.
The master module is cleared so that communication can be executed again. However, the contents of the receive data area will not be cleared.
B105
RST B305
PLS M100
X23 Y0
RST Y23
At completion of clear (X23 ON), the clear request (Y23) turns OFF and at the same time X23 turns OFF.
M100
MOV K8 D0
1-phase input is set. [K18 setting for 2-phase inputs]
MOV K1 D1
Decrement count is set. [K0 setting for increment count]
MOV K1 D2
Coincidence signal output enable specification [K0 setting when disabled]
DMOV K100 D3
Set value specification (D3, D4)
DMOV K50000 D5
Preset value specification (D5, D6)
M9081
LEDA MINI
SUB H0
TO K1 K0 D0 K7
PRC M0 Y0
LEDR
Write by MINI instruction
(7 words of data D0 to D6 are written to the AD61C buffer memory addresses 0 to 6.)
When M0 stays ON for 1 scan at the completion of write, sequence operations such as external display are executed.
Coincidence signal reset command
PLS M101
M101
SET B318
The counter coincidence signal B119 (X19) is reset when B318 (Y18) reset is ON, and external output is reset.
When B119 (X19) is turned OFF, B318 (Y18) is reset.
B119
RST B318
Preset command
PLS M102
M102
SET B319
When B319 (Y19) is turned ON, preset is executed.
At the completion of preset, B11B (X1B) turns ON.
B11B
RST B319
When B11B (X1B) is turned ON, B319 (Y19) turns OFF and at the same time B11B (X1B) turns OFF.
REMARK
(1) Set value and preset value data settings can be executed by other programs. For details, see Section 5.5.3.
(2) See Section 5.5.4 for details about preset example program by external input.


Flow
Sequence Program
Operation
④ Count enable
(Count execution)
⑤ Counter comparison signal processing
⑥ Count coincidence signal output (external output)
⑦ Present value read
⑧ Error detection/ error code read
⑨ Error code reset
Count start command
B31A
CH1's count enable B31A (Y1A) is turned ON.
(When B31A (Y1A) is turned ON, count start/ stop by external input is allowed.
External input ON ····· Stop
External input OFF ····· Start
See Section 3.7 for details.)
B118
B118
Sequence operations such as counter value comparison internal processing, external operation indication/display are executed.
B118 (X18) is ON: Counter value≧set value.
B118 (X18) is OFF: Counter value<set value.
B119
Sequence operations such as counter value coincidence internal processing, external operation indication/display are executed.
• When B119 (X19) is ON, the count coincidence signal is output to the external output terminal (EQU).
• When B119 (X19) is ON, processing operations are executed.
Present value read command M9081
Y0
LEDA MINI
SUB H0
DFRO K1 K14 D20 K1
PRC M1 Y0
LEDR
MINI instruction execution
MINI-S3 master module head I/O number.
upper 2-digit specification
Read from the AD61C (remote terminal No. 1) buffer memory 14, 15 to D20, D21.
MINI instruction reset
Sequence operations of data read to D20, D21 are executed.
REMARK
See Section 5.5.5 for counter present value preset example program.
X24
FROMP H0 K196 D25 K1
Y24
When the S3 error detection (X24) is ON, the error code in the S3 buffer memory K196 (terminal No. 1) is read to D25.
When Y24 is turned ON, X24 turns OFF, then Y24 goes OFF.
Sequence operations such as external display and internal processing of error codes of D25 (terminal No. 1) are executed.
Error code reset command
Y0
PLS M103
MOV K0 D26
M103 M9081
LEDA MINI
SUB H0
TOP K1 K18 D26 K1
PRC M2 Y0
LEDR
MINI instruction execution
MINI-S3 master module head I/O number
upper 2-digit specification
"0" is written as 1 word of data to the AD61C (terminal No. 1) buffer memory 18 (error code) to clear it.
MINI instruction reset

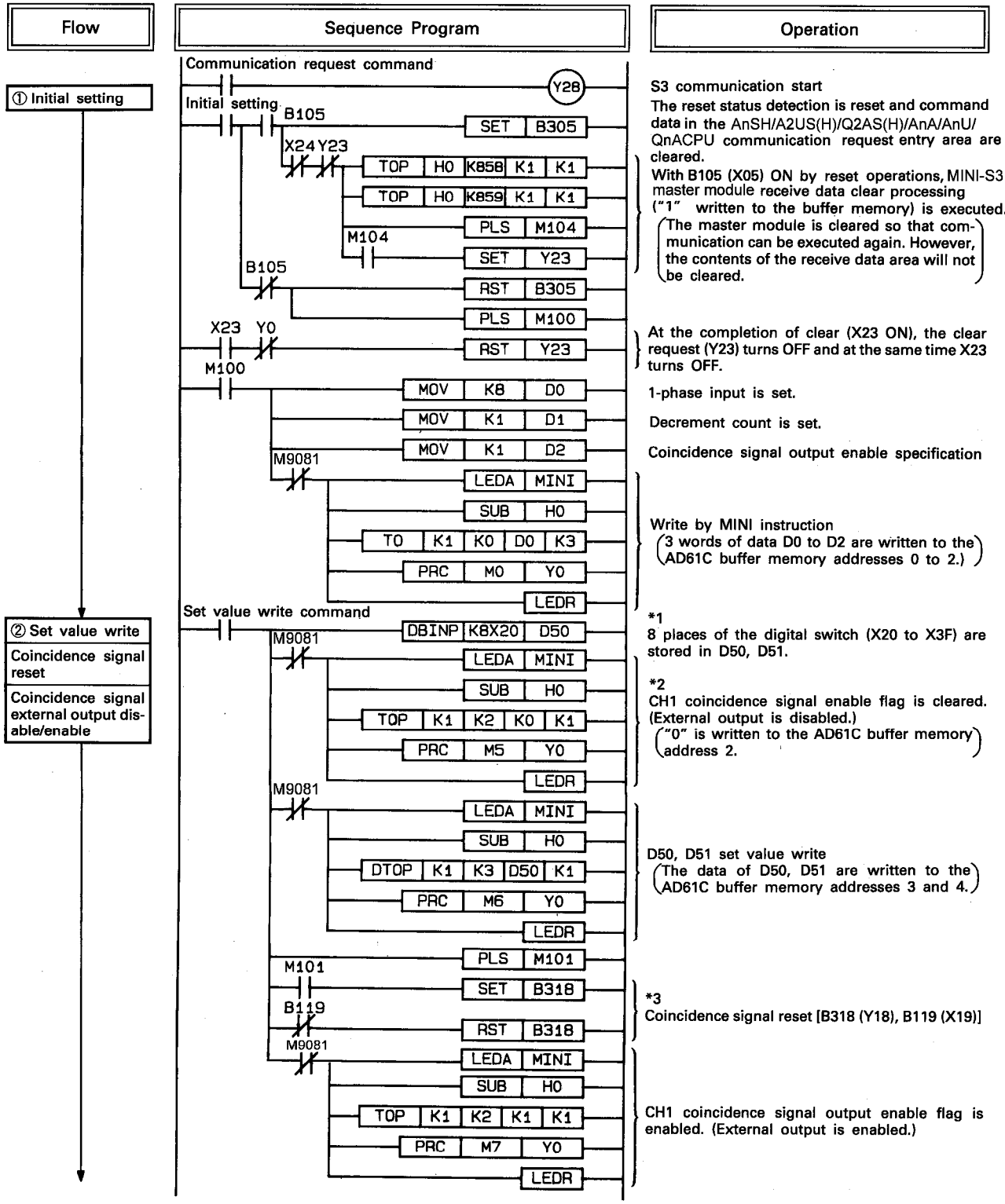
Flow	Sequence Program	Operation
⑩ Data clear processing by reset operations		The allowable communication time is set by the user. AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU command data clear processing when communication is not complete within the set communication time. (uses 2 words of D100, D101)

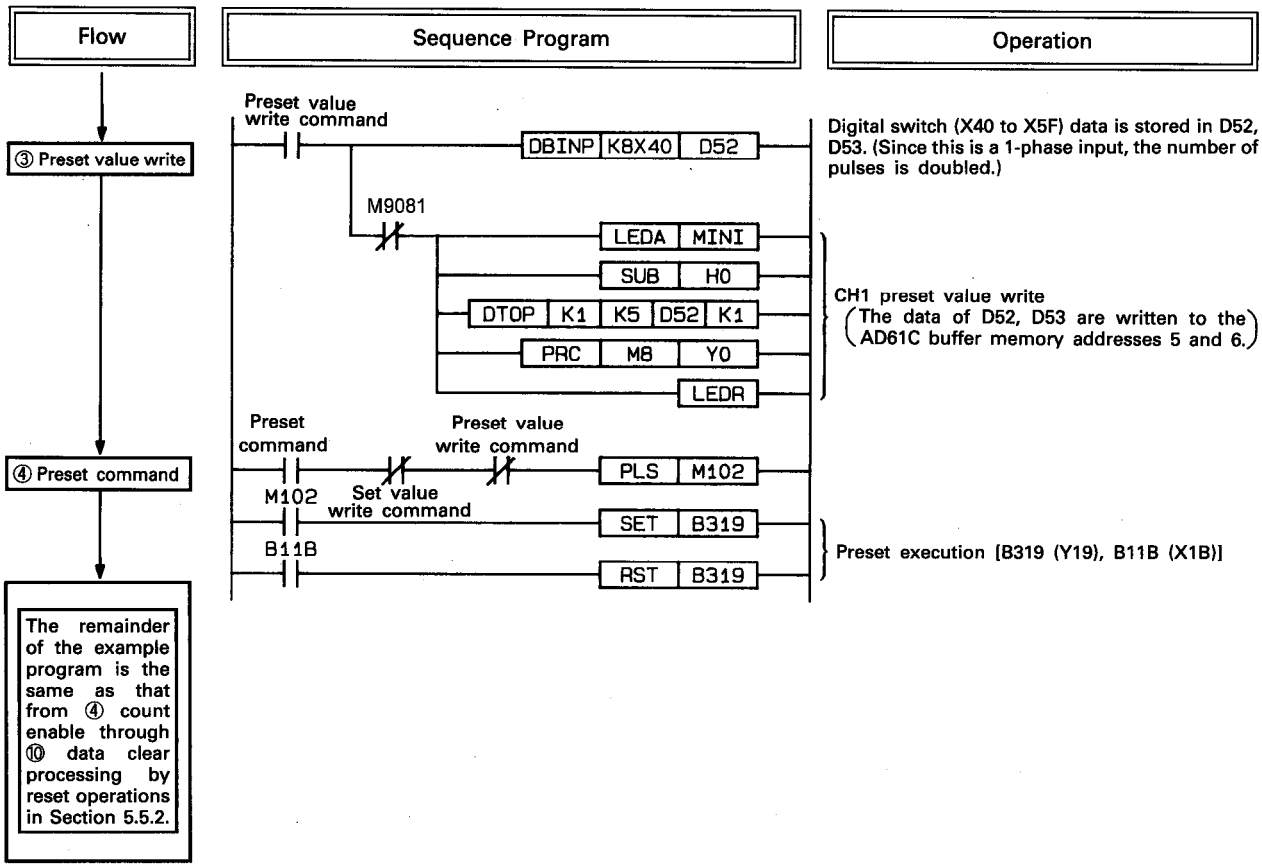
REMARK

When the AD61C reset operations are executed, the buffer memory is cleared. Execute operations from initial setting.

5.5.3 Example program for setting set value and preset value data

Based on the example sequence program of Section 5.5.2, the example program in which the set value and preset value are fetched by the external digital switch and written to the AD61C is shown.
The necessary program is obtained by replacing sequences from (1) initial setting to (3) preset command of Section 5.5.2 with the following sequences.





*1: Set the set value and preset value to double the number of pulses for 1-phase inputs and to 4 times for 2-phase inputs.
*2: Clear the coincidence signal output enable flag before writing set value. (The counter value and set value might coincide when set value data is being written and therefore the coincidence signal should not be output externally.)
*3: Execute coincidence signal reset after set value write and set the coincidence signal output enable flag.

5.5.4 Example preset program by external input

Based on the example sequence programs of Sections 5.5.2 and 5.5.3, an example program in which the [preset command] is executed from the external input terminal (PRST terminal) is shown below.

An example program is obtained by replacing

[(3) preset command] program of Section 5.5.2 and

[(4) preset command] program of Section 5.5.3 with the following sequences.

Flow	Sequence Program	Operation
① Preset command (external input)	External preset request detection reset instruction B11A B11B — SET B31B B11A — RST B31B	When external preset request detection [B11A (X1A)] and preset complete [B11B (X1B)] by external input are ON, CH1 external preset request detection reset [B31B (Y1B)] is turned ON and the external preset request detection signal [B11A (X1A)] is reset: When B11A (X1A) is turned OFF, B31B (Y1B) is reset.

CAUTION

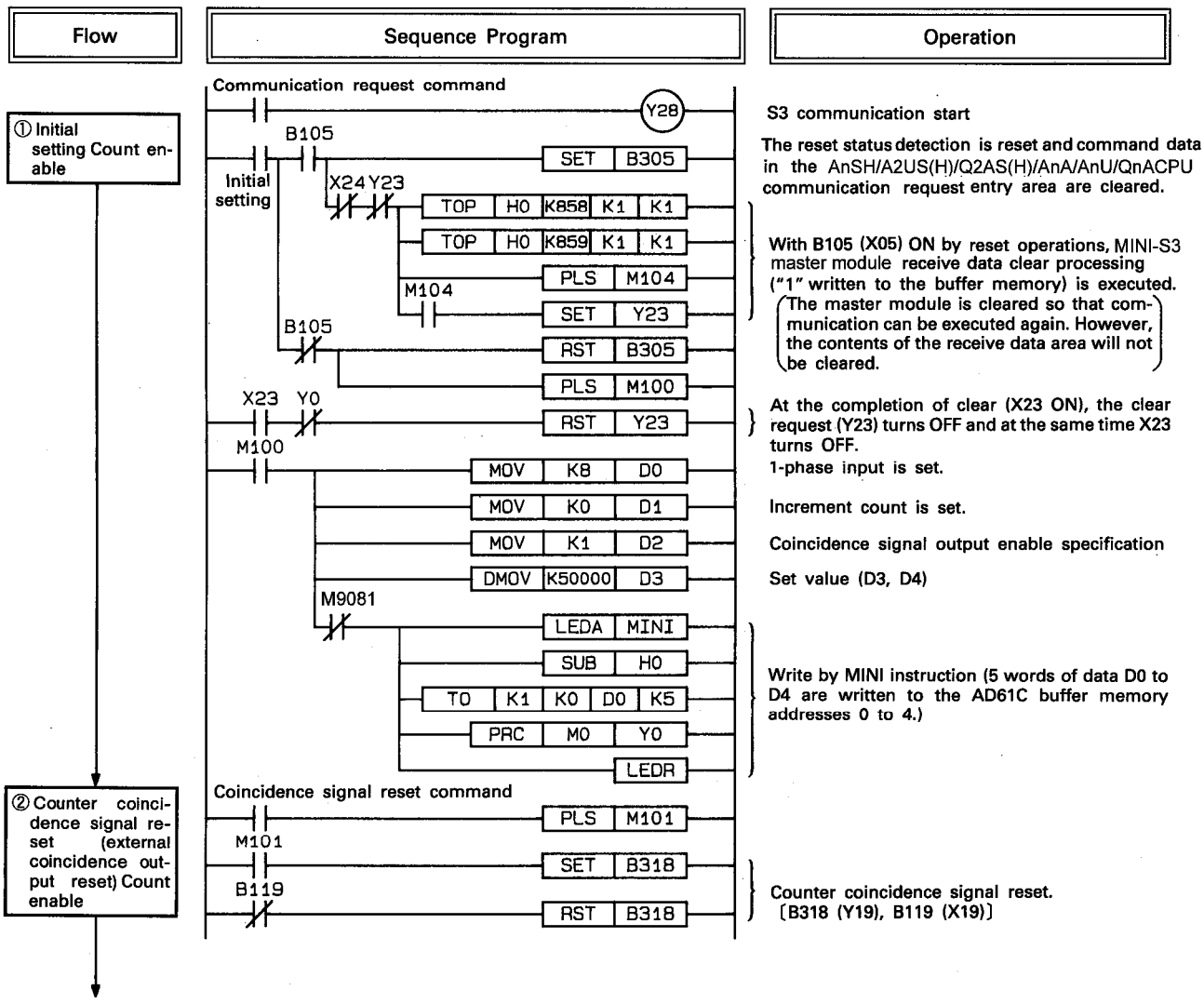
(1) In preset operations by external input, if the preset signal is input to the external terminal (PRST terminal), the external preset request detection B11A (X1A) is turned ON at the preset input's rising edge and the buffer memory internal preset value is preset to the counter value. (See Section 3.4 for details.)
(2) When presetting by external input, reset the external preset request detection each time preset is completed. The next external input is allowed after the external preset request detection is reset.
(3) If the external preset request detection B11A (X1A) is ON, preset by external input and preset command B319 (Y19) by the sequence program cannot operate.
(4) If preset by external input terminal (PRST terminal) is not to be executed, execution of the above program is not necessary.

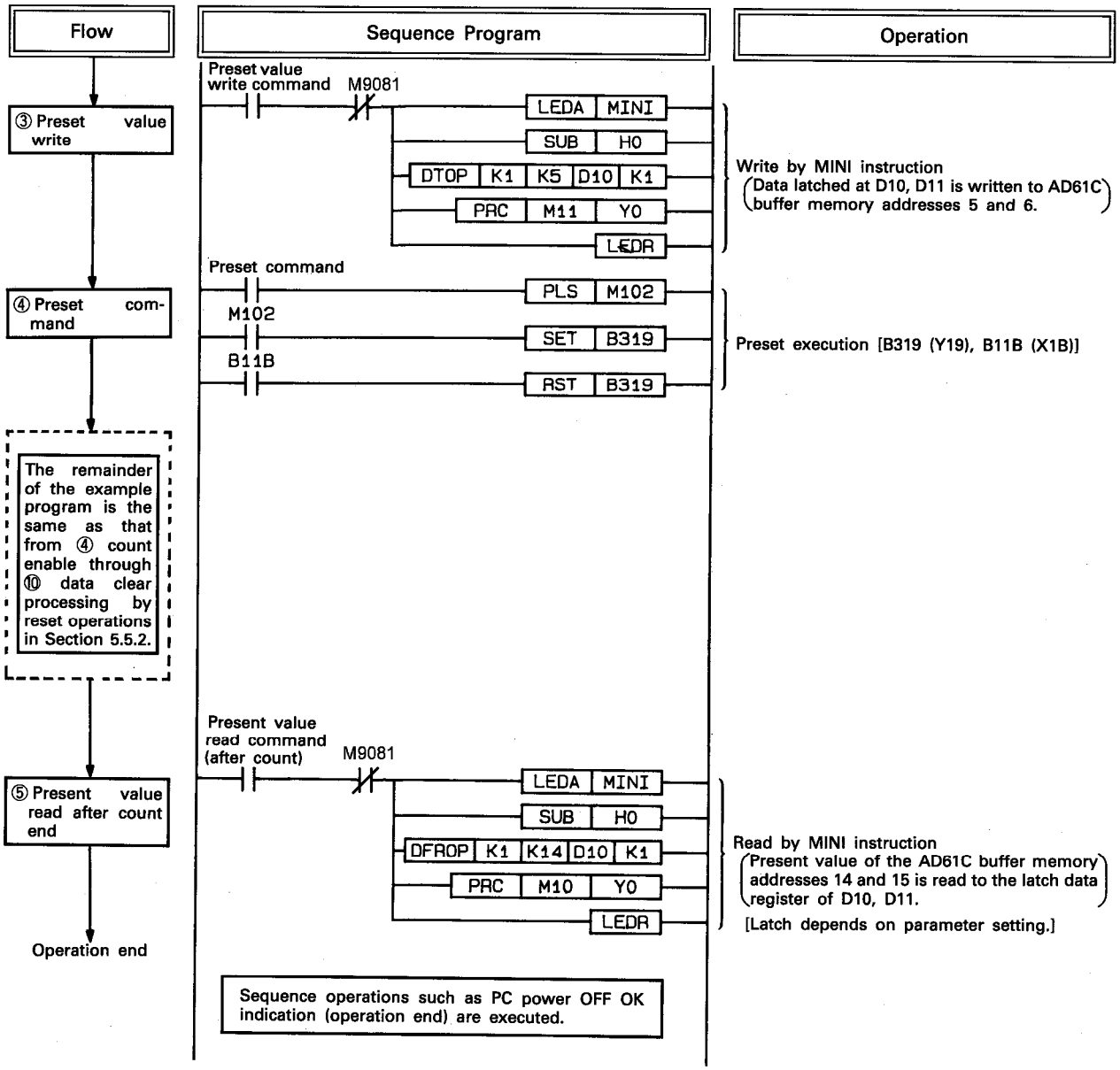
5.5.5 Example program of counter present value preset

An example program in which the counter present value, before the AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU is turned OFF or at count end, is read and counting continues by presetting the read present value before starting the next counting is shown below.

This example program is explained according to the following conditions.

- Settings for the AD61C, MINI-S3 master module and AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU are as described in Section 5.5.
- CH1 is used.
- 1-phase is specified for the pulse input.
- Increment count is specified.
- The external coincidence signal output is enabled.
- The total number of pulses for the set value is 50,000 (25,000×2). The first preset value is 0 (default value).
- The ring counter function is not used.



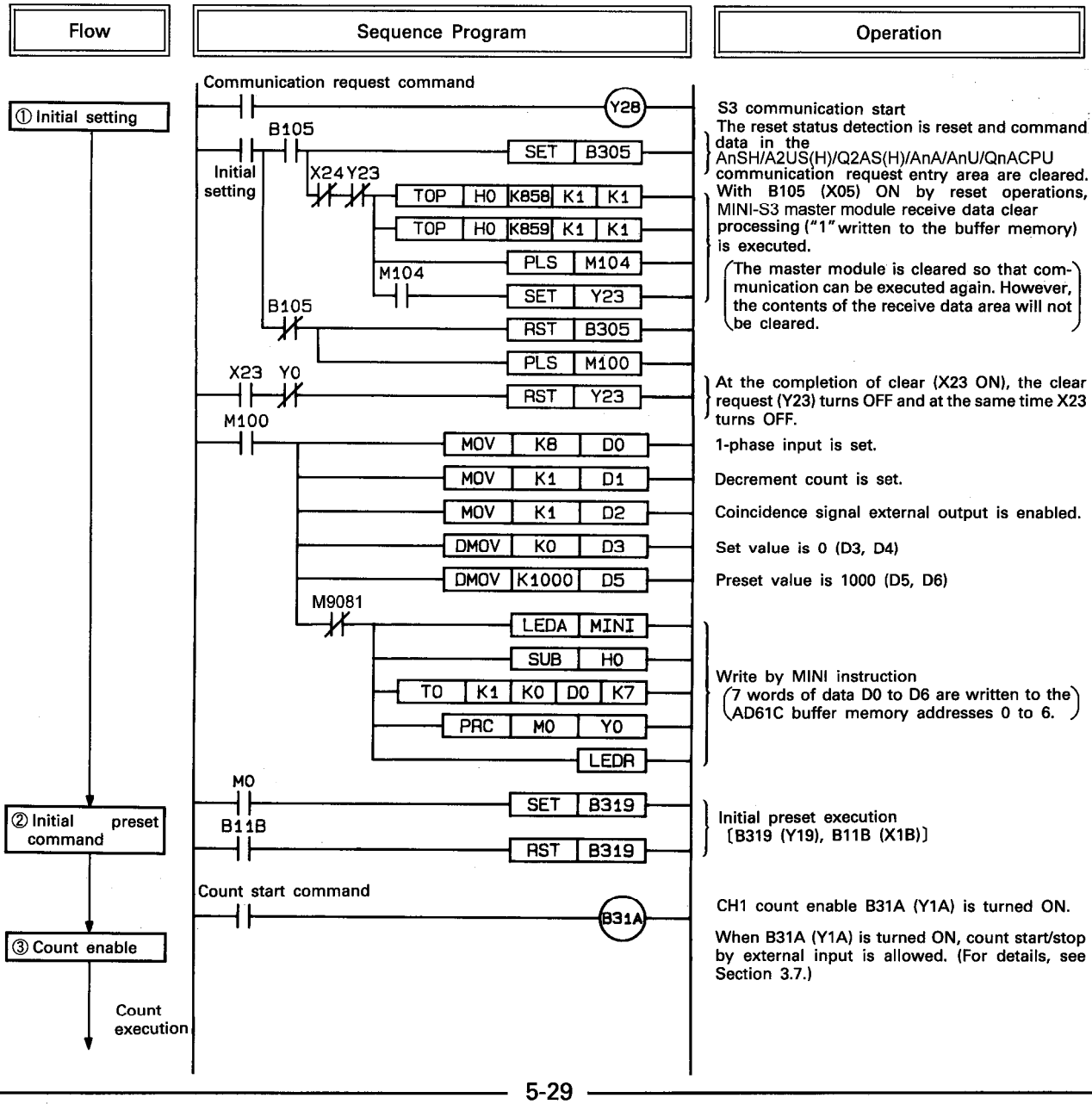

Flow
Sequence Program
Operation
③ Preset value write
④ Preset command
The remainder of the example program is the same as that from ④ count enable through ⑩ data clear processing by reset operations in Section 5.5.2.
⑤ Present value read after count end
Operation end
Preset value write command
M9081
LEDA MINI
SUB H0
DTOP K1 K5 D10 K1
PRC M11 Y0
LEDR
Write by MINI instruction
(Data latched at D10, D11 is written to AD61C buffer memory addresses 5 and 6.)
Preset command
PLS M102
M102
SET B319
B11B
RST B319
Preset execution [B319 (Y19), B11B (X1B)]
Present value read command (after count)
M9081
LEDA MINI
SUB H0
DFROP K1 K14 D10 K1
PRC M10 Y0
LEDR
Read by MINI instruction
(Present value of the AD61C buffer memory addresses 14 and 15 is read to the latch data register of D10, D11.)
[Latch depends on parameter setting.]
Sequence operations such as PC power OFF OK indication (operation end) are executed.

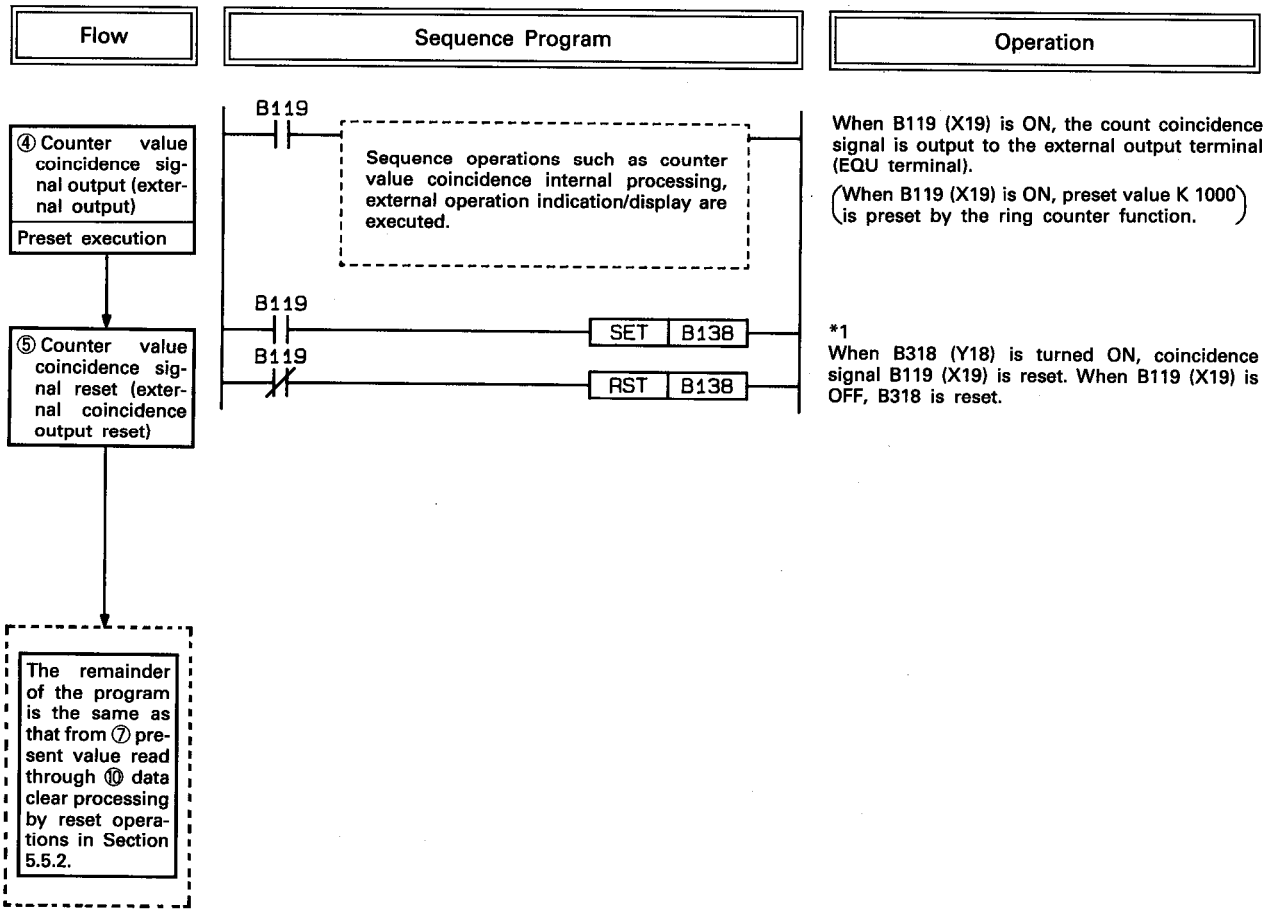
5.5.6 Example program of ring counter function

An example program in which ring count is executed by turning ON the ring counter switch is shown below.

This example program is explained according to the following conditions.

- The settings for the AD61C, MINI-S3 master module , and AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnACPU are as described in Section 5.5.
- CH1 of the AD61C ring counter setting switch is turned ON.
- Only CH1 buffer memory is used and 1-phase is specified for the pulse input.
- Decrement count is specified.
- The external coincidence signal output is enabled.
- Preset is not executed by the external input.
- Count start/stop can be executed by the external input.
- The set value is 0 and the number of pulses for the preset value is 1000 (500×2).





*1: When using the ring counter function, be sure to reset the counter coincidence signal (X19). If X19 is left ON, the next preset cannot be executed.

5.5.7 Programs when 2 channels are used

Programs using 2 channels are explained.

(1) A CH2 example program is created in the same way as CH1 example programs in Sections 5.5.2 to 5.5.6.

(2) The execution content program of CH2 is added as indicated below following the order of the example program Flow.

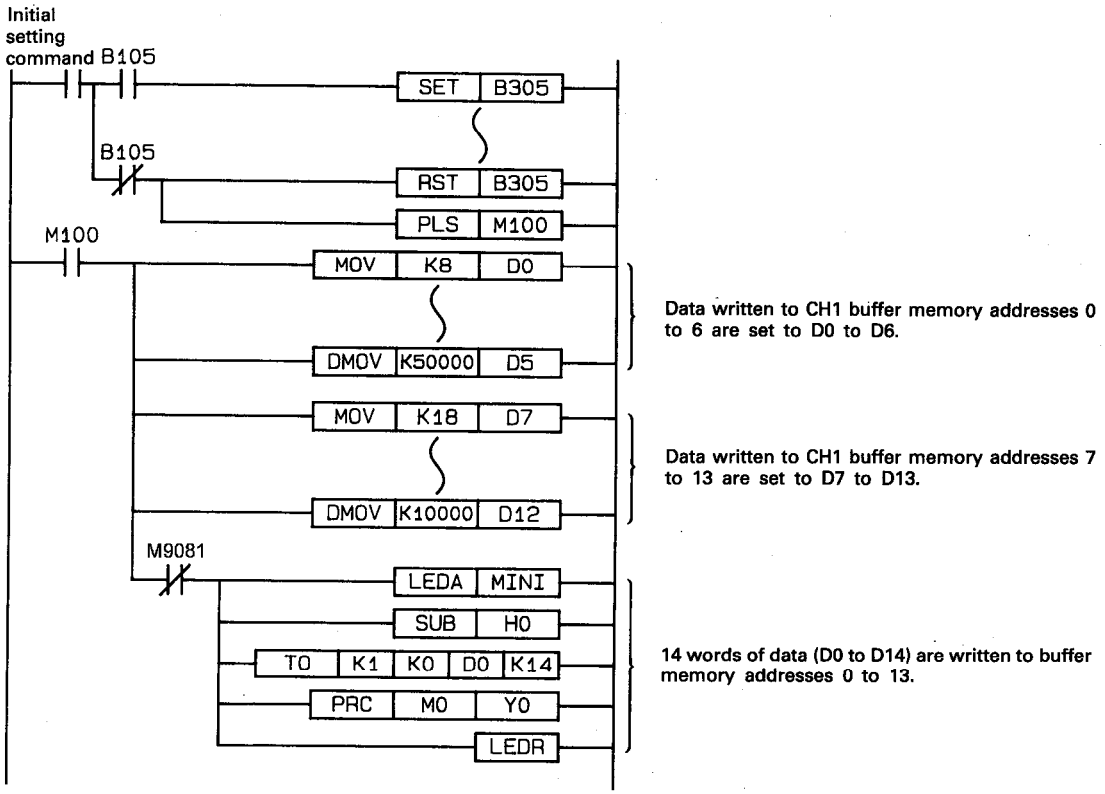
(3) Regarding FROM/TO instructions to be executed for AD61C buffer memory, read/write is possible in batch in the range which the buffer memory can be specified. (See REMARK)

(4) FROM/TO instructions can be used for each buffer memory address.

(5) See Sections 5.3 and 5.4 regarding CH2 I/O signals and buffer memory addresses.

REMARK

• The program which writes CH1 and CH2 initial settings in batch is shown below.



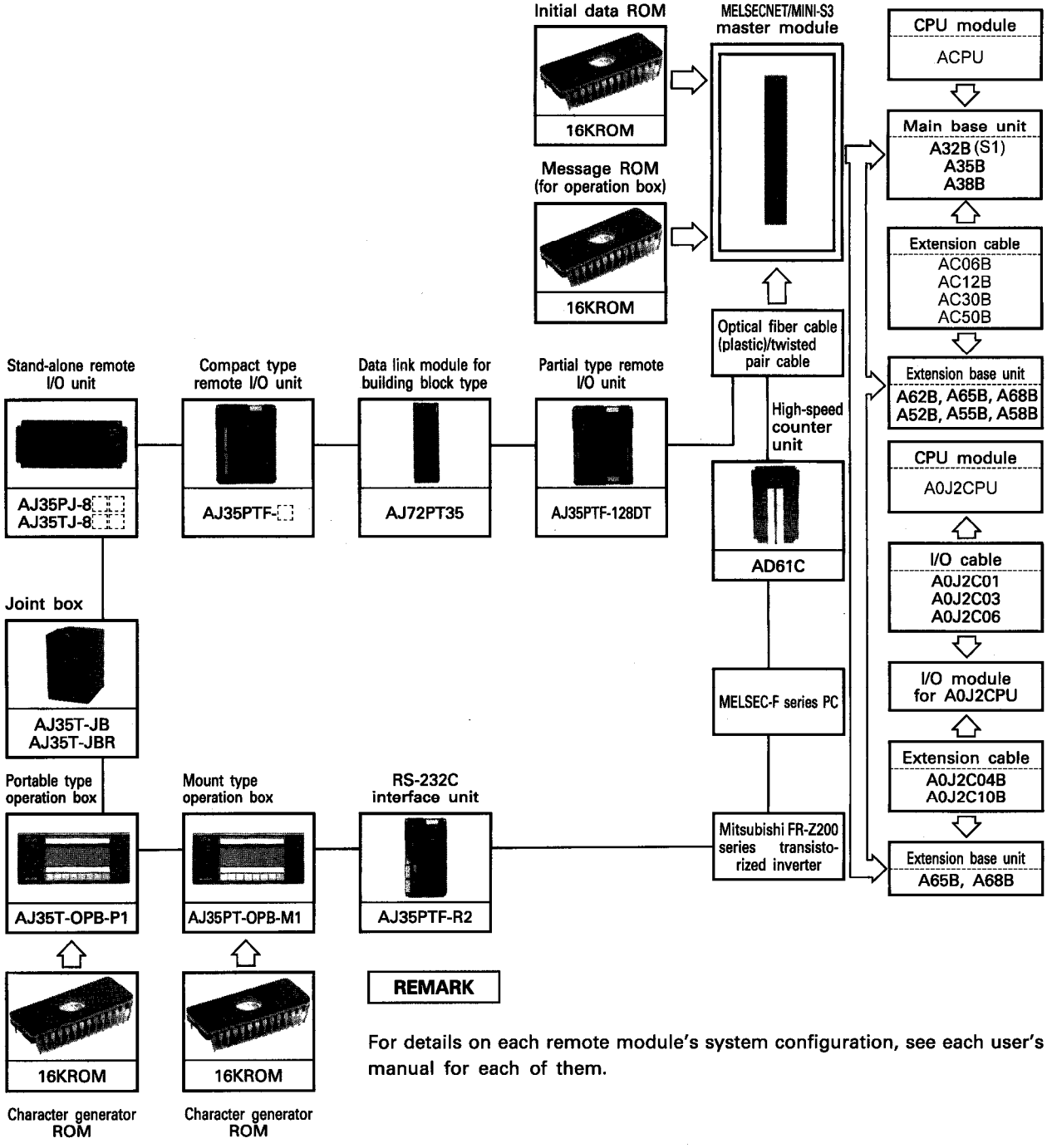
6. ACPU AND MINI-S3 MASTER MODULE LINK

- See Section 4 for link with the A2CCPU.
- See Section 5 for link with the AnACPU/AnUCPU. (Link described in this section can also be used.)

6.1 System Configuration

6.1.1 Overall configuration

The overall configuration of the AD61C using MELSECNET/MINI-S3 is shown below.



REMARK

For details on each remote module's system configuration, see each user's manual for each of them.

6.1.2 Applicable system

The AD61C can be linked to the following CPUs via the MINI-S3 master module.

Applicable models

A0J2HCPU(P21/R21)
A1NCPU(P21(S3)/R21)
A2NCPU(P21(S3)/R21)
A2NCPU(P21/R21)-S1(S4)
A3NCPU(P21(S3)/R21)
A3HCPU(P21(S3)/R21)
A3MCPU(P21/R21)
A2ACPU(P21(S3)/R21)
A2ACPU(P21/R21)-S1(S4)
A3ACPU(P21(S3)/R21)
A2UCPU
A2UCPU-S1
A3UCPU
A4UCPU
A1SJCPU
A1SCPU
A2SCPU
A2USCPU
QA2SCPU

A0J2CPU (P23/R23)
A1CPU (P21/R21)
A2CPU (P21/R21)
A2CPU (P21/R21)-S1
A3CPU (P21/R21)
A1SJHCPU
A1SHCPU
A2SHCPU
A2USHCPU
Q2ASHCPU

The MINI-S3 master module can be loaded into any slot and linked with the AD61C with the exception of (1) and (3) below. The number of device panels is unlimited.

(1) If the AD61C is loaded into an extension base unit (A55B, A58B) without a power supply module, the power capacity may be insufficient. Avoid loading as long as possible. If it is necessary to load, select power supply modules and extension cables with the power capacity of the main base unit's power supply module and extension cable voltage drops in mind. For details, see each CPU user's manual.

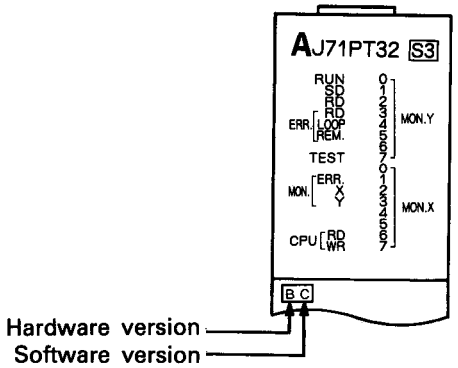
(2) The MINI-S3 master module cannot be loaded into the last slot of the 7th extension of the A3CPU (P21/R21).

(3) In a MELSECNET data link system, loading is possible to both a master station and a local station. The MINI-S3 master module cannot be used for a remote I/O station.

(4) In a MELSECNET/10 network system, the AD61C can be loaded to either a control station or a normal station.
It is not applicable to a remote I/O station.

6.1.3 Cautions on constructing the system

(1) The software version shown below on the front of the AJ71PT32-S3 unit must be "C" or after to use the AD61C. The module of software version "A, B" or "no" software version indication cannot be used.



(2) When using the AD61C in the MELSECNET/MINI-S3 data link system, use twisted pair cables.

(3) Since each AD61C occupies 4 stations (a total of 32 I/O points), be careful when assigning I/O signals.

(4) When using the AD61C, set the MINI-S3 master module as follows.

a) Set the "jumper for mode selection" of the AJ71PT32-S3 to the extension mode (occupying 48 I/O points) of "48."

b) Create the initial data ROM for the MINI-S3 master module extension mode (occupying 48 I/O points) by the SW0GP-MINIP and install it. For remote terminal data setting at creation of the initial ROM, set the AD61C protocol to [4 : MINI STANDARD PROTOCOL].

c) For details, see each of the manuals below.
- AJ71PT32-S3,AJ71T32-S3,A1SJ71PT32-S3,A1SJ71T32-S3 type MELSECNET/MINI-S3 Master Module User's Manual
- SW0GP-MINIP Operating Manual

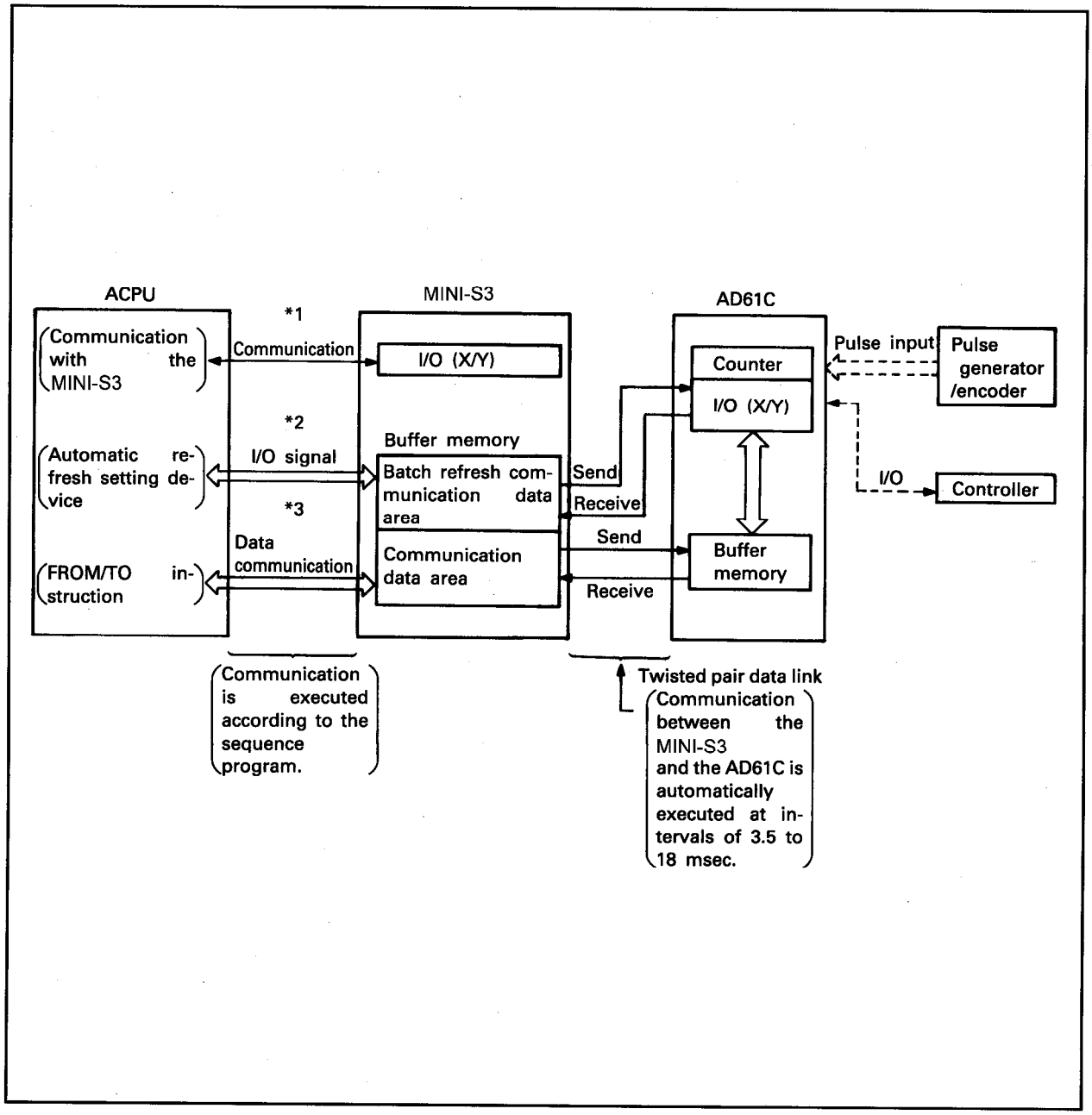
(5) The AD61C requires a 24 VDC power supply.
When supplying power from one power supply to multiple AD61Cs or to the link I/O modules, select cables and perform wiring taking voltage drops into consideration.

To calculate the receiving port voltage, see [REMARK] in Section 4.1.2.

6.2 Data Communication Processing

6.2.1 Communication method

(1) Communication between the AD61C and the ACPU is executed via the MINI-S3 master module' buffer memory. The communication method is shown below.



*1: I/O signal communication between the ACPU and the MINI-S3 master module is executed. (I/O communication processing of communication start, error detection, etc.)

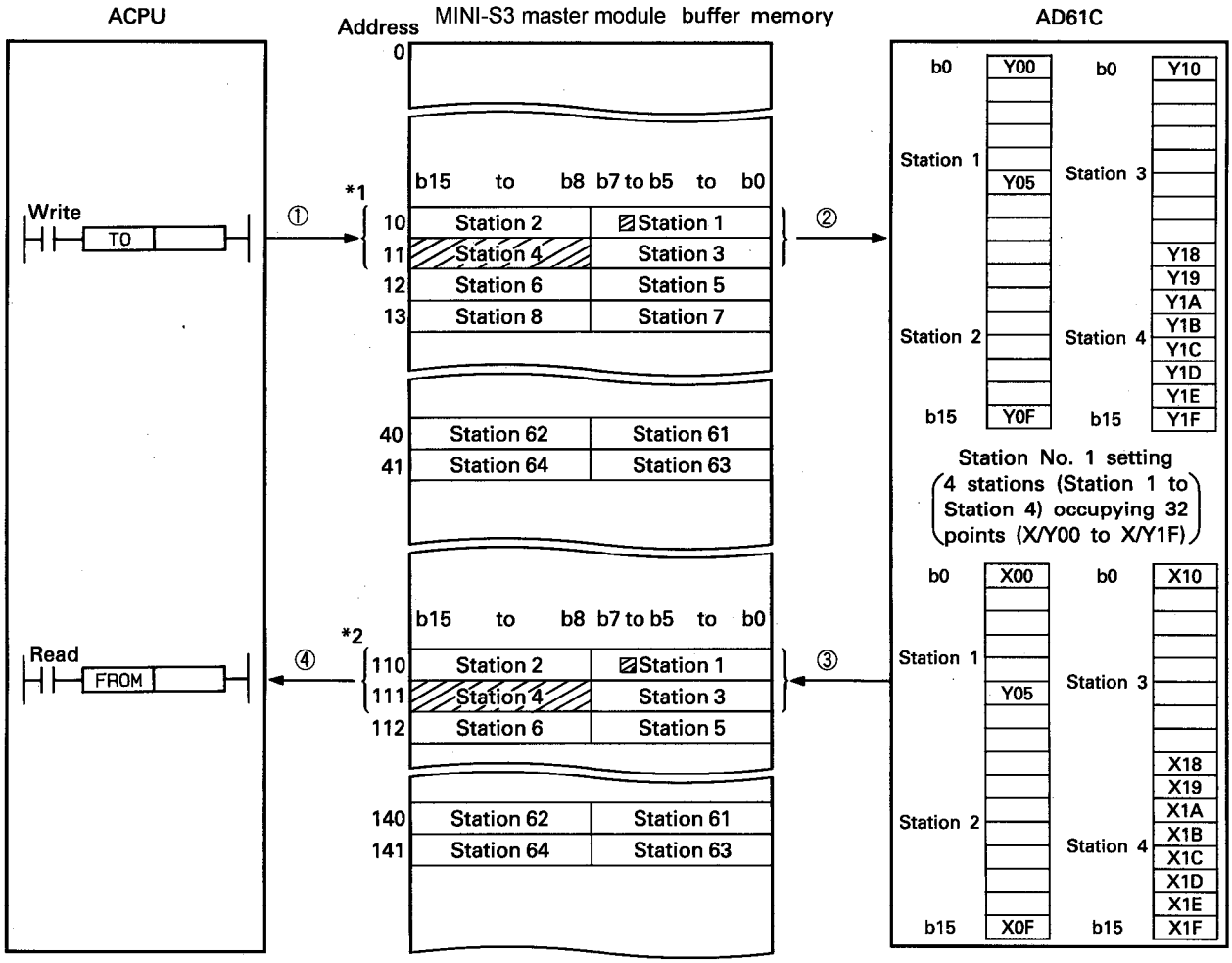
*2: Input signal communication between the ACPU and the MINI-S3 master module , and between the MINI-S3 master module and the AD61C is executed. For details, see "I/O signal processing" in Section 6.2.2.

*3: Data communication between the ACPU and the MINI-S3 master module , and between the MINI-S3 master module and the AD61C is executed. For details, see "buffer memory data processing" in Section 6.2.3.

6.2.2 I/O signal processing

I/O signals (X, Y) of the AD61C to PC CPU are processed via the MINI-S3 master module buffer memory.

(1) The I/O signal processing method between the MINI-S3 master module buffer memory and the AD61C is shown below. (The AD61C station number is set to 01.)



*1: Addresses 10 to 41 ····· Send data area for batch refresh
Addresses 110 to 141 ····· Receive data area for batch refresh

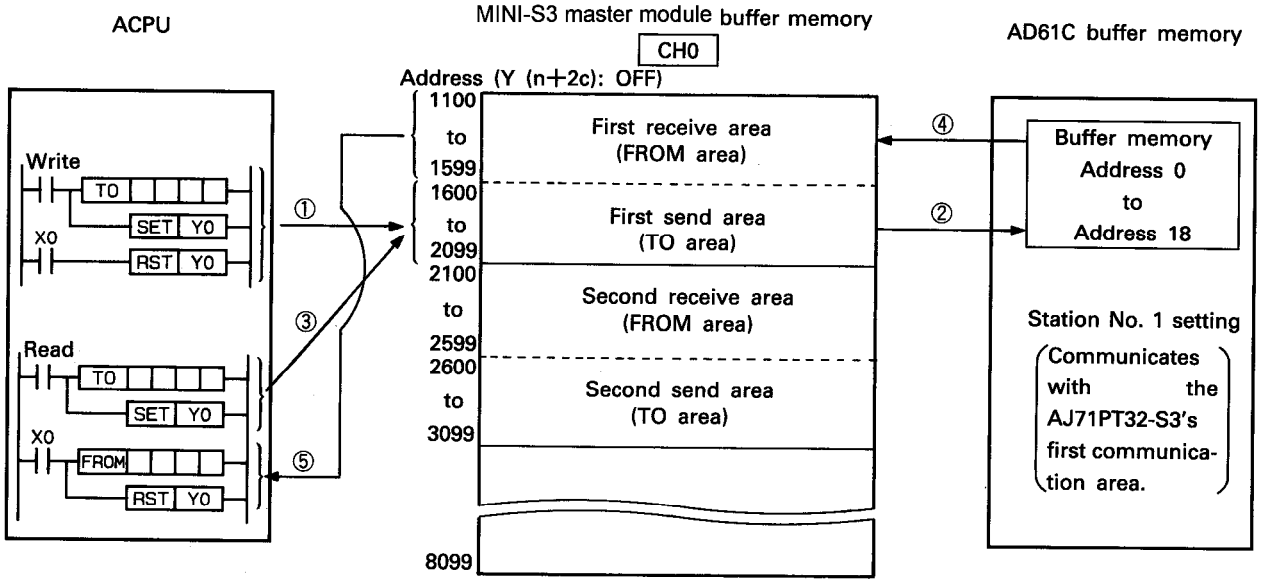
a) Output (Y) signal (communication order from ① to ②)
- By using the sequence program's TO instruction, the ACPU writes data to the MINI-S3 master module batch refresh send data area.
- The MINI-S3 master module writes the send data to the AD61C output signal area.

b) Input (X) signal (communication order from ③ to ④)
- The MINI-S3 master module always communicates with the AD61C and stores the AD61C input signal data in the batch refresh receive data area.
- By using the sequence program's FROM instruction, the ACPU reads data from the MINI-S3 master module receive data area.

6.2.3 Buffer memory data processing

The AD61C buffer memory data are processed by a sequence program via the MINI-S3 master module buffer memory.

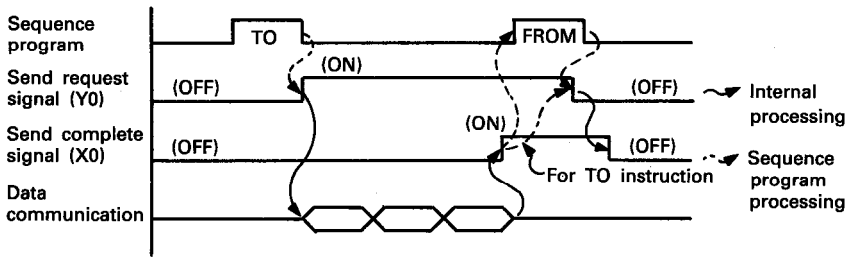
(1) Data processing for MINI-S3 master module and AD61C buffer memory is shown below. Setting is AD61C station number 01, and the communication area of the remote terminal No. 1's 1st unit (by initial ROM).



a) Write to the AD61C buffer memory (communication order from ① to ②)
- By using the sequence program's TO instruction, the ACPU writes data to the MINI-S3 master module send area.
- The MINI-S3 master module writes to the AD61C buffer memory when the send request signal (Y0) is set.

b) Read from the AD61C buffer memory (communication order from ③, ④ to ⑤)
- By using the sequence program's TO instruction, the ACPU writes (read request, head address, number of words to be read) to the MINI-S3 master module send area.
- With the send request signal (Y0) set, the MINI-S3 master module reads the data of the specified number of words to be read from the AD61C buffer memory specified head address according to the send data by the TO instruction.
  Then the MINI-S3 master module stores the data to the receive area and turns ON the send complete signal (X0).
- The receive data are read from the MINI-S3 master module receive area by the sequence program's FROM instruction when the send complete signal (X0) is ON.

c) Processing timing



6.2.4 Processing time

The processing time required to write data to and read data from the AD61C buffer memory is shown below.

(1) Write processing time (T_W)

T_W = {(number of data written) + $\underset{*1}{8}$} × t + $\underset{*2}{10}$ + (ACPU scan time) × 3 [ms]

(2) Read processing time (T_R)

T_R = {(number of data read) + $\underset{*1}{9}$} × t + $\underset{*2}{10}$ + (ACPU scan time) × 3 [ms]

(3) "t" is the I/O refresh time.
It varies according to the number and type of connected remote module stations.
Calculation of the I/O refresh time is shown below.

Mode	Operation Mode Setting	I/O Refresh Time (ms)
Extension mode	Automatic return enable (0)	t=0.66+(0.044×R)+(0.95×B)+(0.95×T)
	Automatic return disable (1)	t=0.54+(0.058×R)+(0.25×B)+(0.95×T)
	Communication stop at error detection (2)	t=0.54+(0.051×R)+(0.25×B)+(0.95×T)

R: Total number of remote stations
B: Number of AJ35PTF-128DTs
T: Number of remote terminal units

POINT

(1) Count start/stop by external input, preset, and the counter coincidence signal by external output respond in less than 10 msec.
(2) To increase the processing time responsiveness of sequence operations, use external I/O signals.

REMARK

1) *1: Number of system data communications between master module and AD61C
2) *2: A61C internal processing time

6.3 I/O Signals to the Sequencer CPU

6.3.1 AD61C I/O signals

I/O signals when the AD61C station No. is 01 (X/Y00 to X/Y1F) are shown below.

(1) Input signals (Signal direction: AD61C → ACPU)

Device No.		Signal	Operation Status
CH1	CH2		
X00 to X04		(Unused)	—
X05		Reset status detection	• Latched upon AD61C power application or when reset switch is ON. • When reset status detection reset (Y05) is turned ON, X05 turns OFF.
X06 to X17		(Unused)	—
X18	X1C	CH1/CH2 counter value comparison	• ON: Counter value=set value. • OFF: Counter value<set value.
X19	X1D	CH1/CH2 counter value coincidence	• Latched if counter value=set value. • When the coincidence signal reset command (Y18, Y1C) is turned ON, X19 and X1D turn OFF.
X1A	X1E	CH1/CH2 external preset request detection	• Latched if an external preset request is given. • When the external preset request detection reset (Y1B, Y1F) is turned ON, X1A and X1E turn OFF.
X1B	X1F	CH1/CH2 preset completion	• Latched at the completion of preset when the preset command (Y19, Y1D) is ON. • When the preset command (Y19, Y1D) is turned OFF, X1B and X1F turns OFF.

(2) Output signals (Signal direction: ACPU → AD61C)

Device No.		Signal	Operation Status
CH1	CH2		
Y00 to Y04		(Unused)	—
Y05		Reset of reset status detection	• When reset status detection reset (Y05) is turned ON, preset status detection (X05) turns OFF. • When X05 is OFF, Y05 turns OFF.
Y06 to Y17		(Unused)	—
Y18	Y1C	CH1/CH2 coincidence signal reset command	• If the coincidence signal reset command (Y18, Y1C) is turned ON, the counter coincidence signal (X19, X1D) and the external output (EQU) turn OFF. • When X19 and X1D are OFF, Y18 and Y1C turn OFF.
Y19	Y1D	CH1/CH2 preset command	• At the rising edge from OFF to ON of the preset command (Y19, Y1D), the preset value is written. • At the completion of preset (X1B, X1F), Y19 and Y1D turn OFF.
Y1A	Y1E	CH1/CH2 count enable	• When count enable (Y1A, Y1E) is turned ON, counting is enabled. • When count enable (Y1A, Y1E) is turned OFF, counting is disabled.
Y1B	Y1F	CH1/CH2 external preset request detection reset	• When external preset request detection reset (Y1B, Y1F) is turned ON, external preset request detection (X1A, X1E) turns OFF. • When X1A and X1E are OFF, Y1B and Y1F turn OFF.

6.3.2 MINI-S3 master module I/O signals

I/O signals between the MINI-S3 master module and the ACPU in the extension mode are used when accessing the AD61C buffer memory.
For details about the I/O signals, see the MELSECNET/MINI-S3 Master Module User's Manual.
The list of I/O signals in the extension mode is shown below. "n" in the Device No. column of the table is the master module head I/O number. It is determined by the number of I/O points of the I/O modules loaded into the master module's front slot and by the master module's position.

Example: When the master unit head I/O number is "X/Y20"
X (n+0) to X (n+2F)=X20 to X4F
Y (n+0) to Y (n+2F)=Y20 to Y4F

Device No.	Signal		Device No.	Signal	
X (n+0)	Send complete signal	For remote terminal unit No. 1	Y (n+0)	Send complete signal	For remote terminal unit No. 1
X (n+1)	Read request signal		Y (n+1)	Read request signal	
X (n+2)	Send complete signal	For remote terminal unit No. 2	Y (n+2)	Send complete signal	For remote terminal unit No. 2
X (n+3)	Read request signal		Y (n+3)	Read request signal	
X (n+4)	Send complete signal	For remote terminal unit No. 3	Y (n+4)	Send complete signal	For remote terminal unit No. 3
X (n+5)	Read request signal		Y (n+5)	Read request signal	
X (n+6)	Send complete signal	For remote terminal unit No. 4	Y (n+6)	Send complete signal	For remote terminal unit No. 4
X (n+7)	Read request signal		Y (n+7)	Read request signal	
X (n+8)	Send complete signal	For remote terminal unit No. 5	Y (n+8)	Send complete signal	For remote terminal unit No. 5
X (n+9)	Read request signal		Y (n+9)	Read request signal	
X (n+A)	Send complete signal	For remote terminal unit No. 6	Y (n+A)	Send complete signal	For remote terminal unit No. 6
X (n+B)	Read request signal		Y (n+B)	Read request signal	
X (n+C)	Send complete signal	For remote terminal unit No. 7	Y (n+C)	Send complete signal	For remote terminal unit No. 7
X (n+D)	Read request signal		Y (n+D)	Read request signal	
X (n+E)	Send complete signal	For remote terminal unit No. 8	Y (n+E)	Send complete signal	For remote terminal unit No. 8
X (n+F)	Read request signal		Y (n+F)	Read request signal	
X (n+10)	Send complete signal	For remote terminal unit No. 9	Y (n+10)	Send complete signal	For remote terminal unit No. 9
X (n+11)	Read request signal		Y (n+11)	Read request signal	
X (n+12)	Send complete signal	For remote terminal unit No. 10	Y (n+12)	Send complete signal	For remote terminal unit No. 10
X (n+13)	Read request signal		Y (n+13)	Read request signal	
X (n+14)	Send complete signal	For remote terminal unit No. 11	Y (n+14)	Send complete signal	For remote terminal unit No. 11
X (n+15)	Read request signal		Y (n+15)	Read request signal	
X (n+16)	Send complete signal	For remote terminal unit No. 12	Y (n+16)	Send complete signal	For remote terminal unit No. 12
X (n+17)	Read request signal		Y (n+17)	Read request signal	
X (n+18)	Send complete signal	For remote terminal unit No. 13	Y (n+18)	Send complete signal	For remote terminal unit No. 13
X (n+19)	Read request signal		Y (n+19)	Read request signal	
X (n+1A)	Send complete signal	For remote terminal unit No. 14	Y (n+1A)	Send complete signal	For remote terminal unit No. 14
X (n+1B)	Read request signal		Y (n+1B)	Read request signal	
X (n+1C)	(Unused)		Y (n+1C)	(Unused)	
X (n+1D)			Y (n+1D)		
X (n+1E)			Y (n+1E)		
X (n+1F)			Y (n+1F)		
X (n+20)	Hardware error		Y (n+20)		
X (n+21)	MINI-S3 link communication in progress		Y (n+21)		
X (n+22)	(Unused)		Y (n+22)		
X (n+23)	Receive data clear complete (for the AJ35PTF-R2)		Y (n+23)	Receive data clear request (for the AJ35PTF-R2)	
X (n+24)	Remote terminal unit error detection		Y (n+24)	Remote terminal unit error detection reset	
X (n+25)	Test mode		Y (n+25)	(Unused)	
X (n+26)	MINI-S3 link error detection		Y (n+26)		
X (n+27)	MINI-S3 link communication error		Y (n+27)		
X (n+28)	ROM error		Y (n+28)	MINI-S3 link communication start	
X (n+29)	(Unused)		Y (n+29)	(Unused)	
X (n+2A)			Y (n+2A)	FROM/TO instruction response specification	
X (n+2B)			Y (n+2B)	Error station data clear specification	
X (n+2C)			Y (n+2C)	Buffer memory channel switching	
X (n+2D)			Y (n+2D)	Error reset	
X (n+2E)			Y (n+2E)	(Unused)	
X (n+2F)			Y (n+2F)		

I/O signal List in the Extension Mode

6.4 Buffer Memory Assignment

6.4.1 AD61C buffer memory

The AD61C does not have battery backup. When power is turned OFF or when the AD61C is reset, the buffer memory will be cleared (initialized).
When the ACPU is reset, the coincidence signal output enable flag of CH1, CH2 (CH1=2, CH2=9) will be initialized.

Memory buffer assignment is shown below.

Address (decimal)	Name	Description	Read/Write (FROM/TO)	Initial Value
0	CH1 mode register	• 1 or 2-phase input specification • See (1) for data to be specified.	TO (FROM)	18
1	CH1 operation count specification	• Increment/decrement specification • See (2) for data to be specified.	TO	0
2	CH1 coincidence signal output enable flag	• Specification when coincidence signal is output to outside • See (3) for data to be specified.	TO	0
3	CH1 set value	• Storage of higher and middle digit data of set value	TO (FROM)	
4		• Storage of lower digit data of set value		
5	CH1 preset value	• Storage of higher and middle digit data of preset value	TO	0
6		• Storage of lower digit data of preset value		
7	CH2 mode register	• 1 or 2-phase input specification • See (1) for data specified.	TO (FROM)	18
8	CH2 operation count specification	• Increment/decrement specification • See (2) for data specified.	TO	0
9	CH2 coincidence signal output enable flag	• Specification when coincidence signal is output to outside • See (3) for data to be specified.	TO	0
10	CH2 set value	• Storage of higher and middle digit data of set value	TO (FROM)	
11		• Storage of lower digit data of set value		
12	CH2 preset value	• Storage of higher and middle digit data of preset value	TO	0
13		• Storage of lower digit data of preset value		
14	CH1 present value	• Storage of higher and middle digit data of present value	FROM	
15		• Storage of lower digit data of present value		
16	CH2 present value	• Storage of higher and middle digit data of present value		
17		• Storage of lower digit data of present value		
18	Error code	• Storage of the error code of the first error		

(1) Mode register's written data (CH1=0, CH2=7)

	Written data	Initial value
Used by 1-phase	8	18 (2-phase)
Used by 2-phase	18	

(Caution)
If data other than 8, 18 are written, an error occurs. The error code will be set to address 18 and counting controlled by the initial value.

(2) Decrement count command's written data (CH1=1, CH2=8)
Valid only for 1-phase inputs.

	Written data	Initial value
Decrement count specification	1	0 (Increment)
Increment count specification	0	

(Caution)
Data written are valid only for the lower 1 bit. The upper 15 bits will be ignored.

(3) Coincidence signal output enable flag's written data (CH1=2, CH2=9)

	Written data	Initial value
Enable	1	0 (disabled)
Disable	0	

(Caution)
Written data are valid only for the lower 1 bit. The upper 15 bits will be ignored.

POINT

Since increment/decrement count of phases A and B of a 2-phase input will automatically be determined, the contents of the buffer memory will be invalid.

6.4.2 MINI-S3 master module buffer memory

There are communication (send/receive) data addresses for the MINI-S3 master module buffer memory according to dedicated read/write instructions between the MINI-S3 master module and the ACPU.
The assignment of buffer memory addresses which automatically communicate with the AD61C is shown below.
For details of the buffer memory, see the MELSECNET/MINI-S3 Master Module User's Manual.

	Address (decimal)		Content	PC CPU Read/write Enable/disable
	0	Total number of remote stations	The range of the station numbers of all connected remote units is set.	Read/write enable
	1	Number of retries	The number of retries at communication error occurrence is set.	
		(Unused)	—	
	4	Line error check	Used to confirm line faulty areas.	
		(Unused)	—	
*1	10 to 41	Batch refresh send data	Data output to the batch refresh type remote I/O module are written.	
		(Unused)	—	—
	70 to 77	Remote unit's card data	Each connected remote unit's type is stored.	Read only
		(Unused)	—	—
	90 to 93	Accumulation faulty station detection	Station numbers of remote units which are in communication error are stored. (Detection status is retained until reset.)	Read/write enable
		(Unused)	—	—
	100 to 103	Faulty station detection	Station number of remote unit which is in communication error is stored. (Communication status is always updated.)	Read only
		(Unused)	—	
	107	Communication error code	The cause of the MINI-S3 link communication error signal being ON is stored.	
	108	Error detection code	The accumulated number of times the MINI-S3 link error detection turns ON is stored.	
		(Unused)	—	
*2	110 to 141	Batch refresh receive data	Input data from batch refresh type remote I/O module are stored.	
		(Unused)	—	
	160	Line error retry counter	The number of executions of retry processing when communication with all remote units is disabled by line error is stored.	
	161 to 192	Retry counter	The number of times retry processing to faulty stations is executed is stored.	
		(Unused)	—	
*3	195	Remote terminal unit faulty stations	The station number of the remote terminal unit with which an error has occurred is stored.	
	196 to 209	Remote terminal unit error code	The cause of the remote terminal unit error detection signal [X (n+24)] being ON is stored.	
		(Unused)	—	—
	250 to 282	Partial refresh station	Partial refresh type remote I/O module station No. and specification of the number of digits are written.	Read/write enable
		(Unused)	—	
	300 to 363	Partial refresh send data	Data output to the partial refresh type remote I/O module are written.	
		(Unused)	—	
	598	Partial refresh accumulation input error detection	Partial refresh type remote I/O module's input data received faulty station is stored. (Detection status is retained until reset.)	
	599	Partial refresh input error detection	Partial refresh type remote I/O module's input data received faulty station is stored. (Communication status is always undated.)	
	600 to 663	Partial refresh receive data	Partial refresh type remote I/O module's input data are stored.	Read only

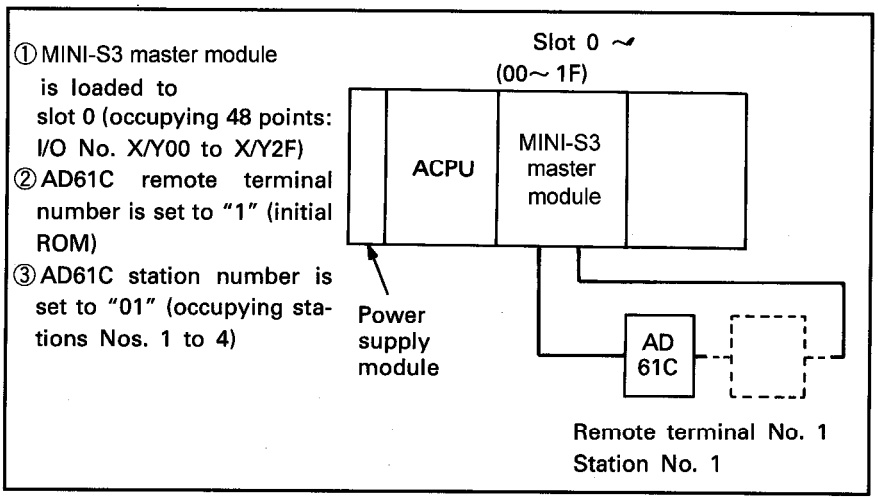
*1: Output signal data write area to the AD61C
*2: Store area of the input signal data from the AD61C
*3: Area which stores station number and error code when an AD61C error occurs. (See Section 8.1 for error codes.)

	Address (decimal)			Content	PC CPU Read/write Enable/disable
*4	858	Receive data clear specification		The AJ35PTF-R2 station number which executes receive data clear by the receive data clear request signal [Y (n+23)] is specified.	Read/write enable
	859	Receive data clear range specification		The receive buffer which is cleared when the receive data clear is executed by the receive data clear request signal [Y (n+23)] is specified.	
	860 to 929	No-protocol mode parameter		Parameters when using the AJ35PTF-R2 in a no-protocol mode are set.	
	930 to 1099	(Unused)		—	—
		CH0	CH1		
*5	1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8	Send data to the remote terminal unit write area, or, receive data from the remote terminal unit store area.	Read/write enable
	2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9		
	3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10		
	4100 to 5099	Communication area for remote terminal No. 4	Communication area for remote terminal No. 11		
	5100 to 6099	Communication area for remote terminal No. 5	Communication area for remote terminal No. 12		
	6100 to 7099	Communication area for remote terminal No. 6	Communication area for remote terminal No. 13		
	7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14		
		[Y (n+2C) at OFF]	[Y (n+2C) at ON]		

*4: Clear processing area of receive data by the AD61C reset operation
*5: Buffer memory area for AD61C data transfer (1st module to 14th module)

6.5 Programming

Programming is explained below under the following setting conditions of ACPU, MINI-S3 master module, and AD61C.



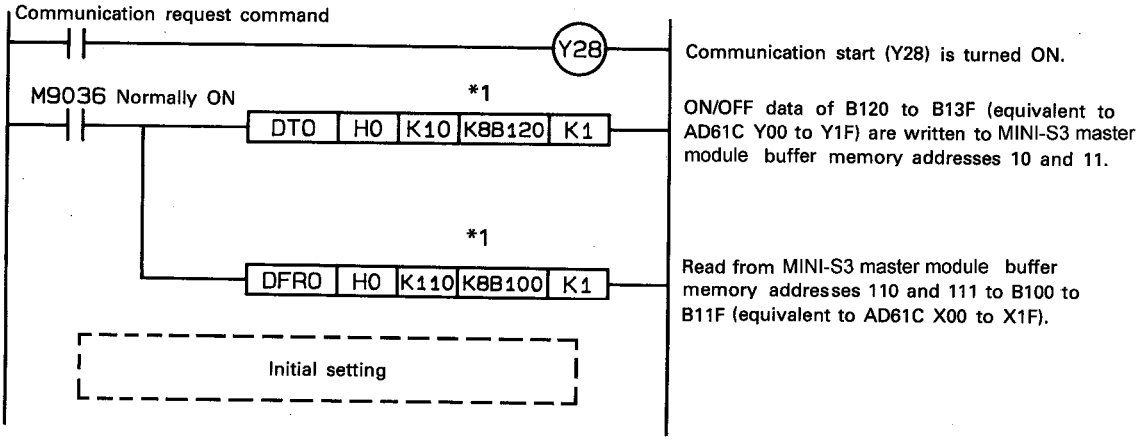
REMARKS

When the MINI-S3 master module is loaded into slot 0 of the extension base of A0J2H/A0J2CPU, the upper 2 digits of the FROM/TO instruction head I/O number will be H10 because 64-point I/O numbers (100 to 13F) are occupied.

6.5.1 Basic programs

Basic programs to the MINI-S3 master module are explained below.

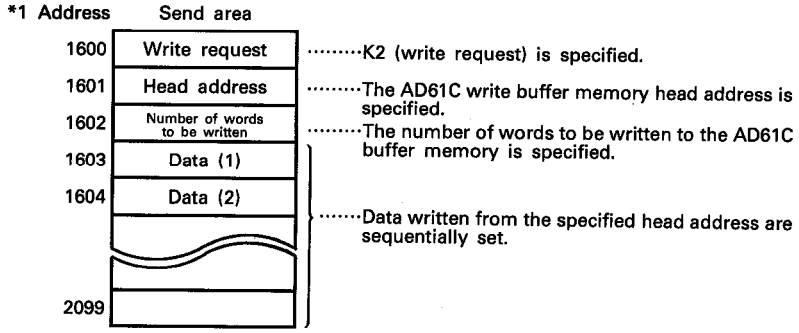
(1) I/O signal processing program



*1 : Since the A0J2CPU (P23/R23) and A1 to A3CPU (P21/R21) cannot use bit devices, use data register (D) to execute read/write.

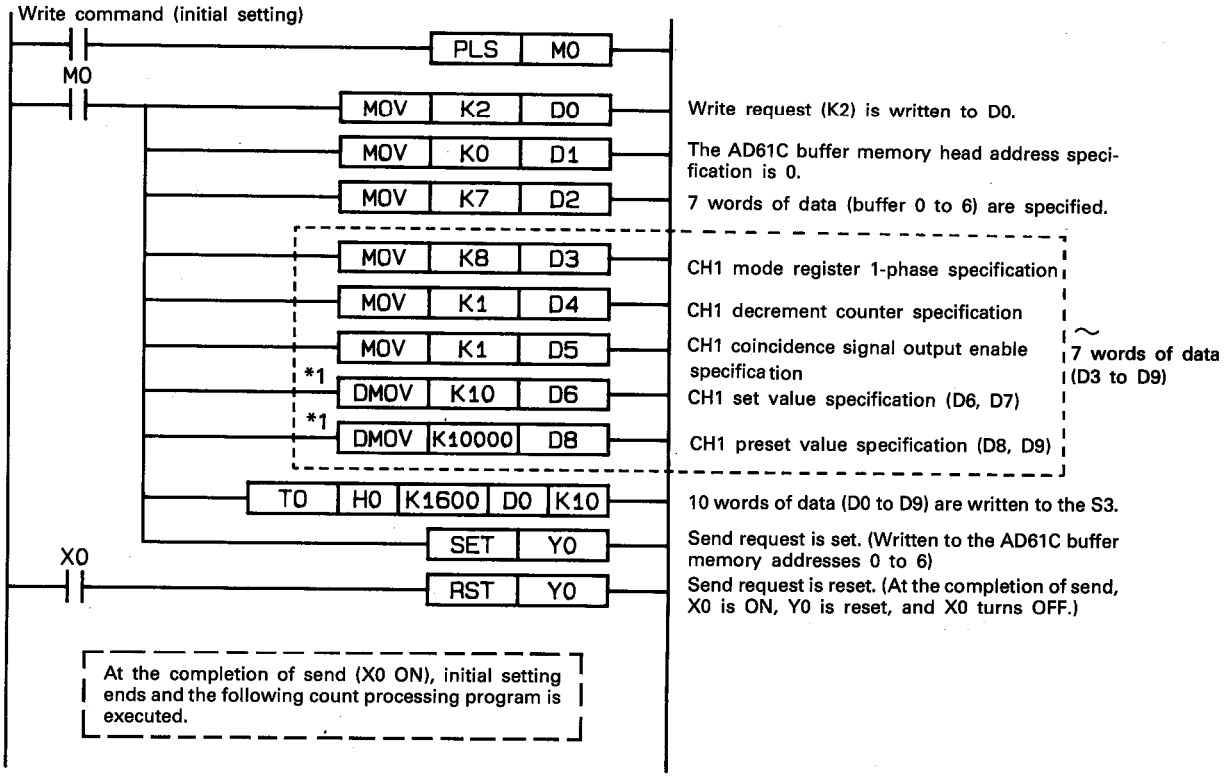
(2) Program to write to the buffer memory

(a) MINI-S3 master module buffer memory write area details (1st unit's address)



*1 : Data content from the head addresses of units 2 to 14 is the same.

(b) Write program



*1 : Since there is no DMOV instruction for the A0J2CPU (P23/R23), use the MOV instruction.

(3) Read program from the buffer memory

a) MINI-S3 master module buffer memory write and read area details (1st unit's address)

*1

Address	(Send area)	
1600	Read request	····· K1 (read request) is specified.
1601	Head address	····· The AD61C buffer memory head address is specified.
1602	Number of words to be read	····· The number of words to be read from the AD61C is specified.
		····· (Not set)

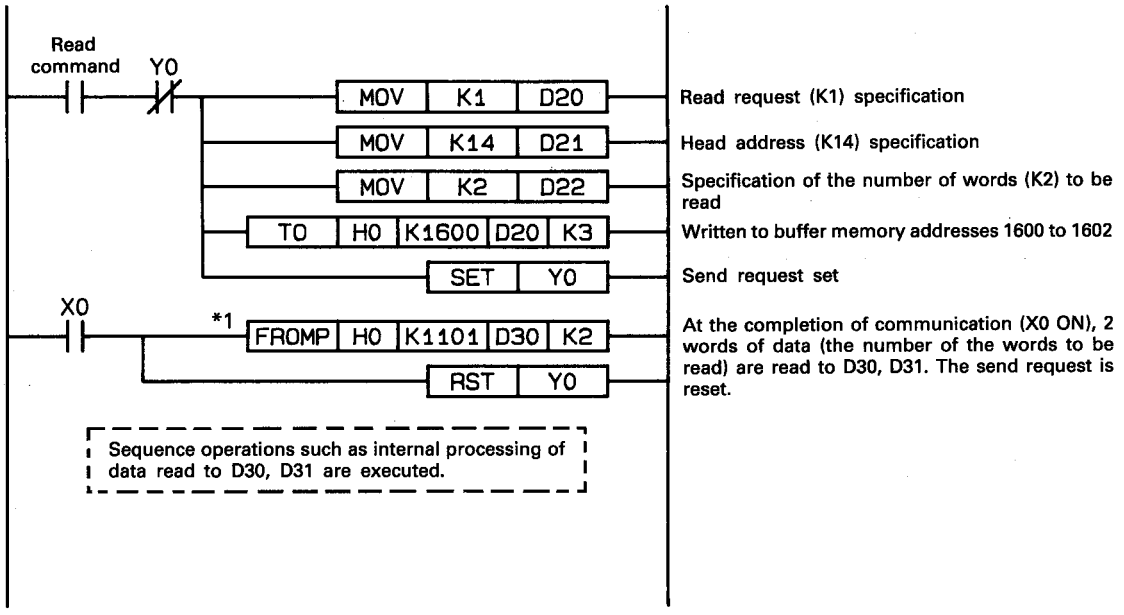
*2

Address	(Receive area)	
1100	Number of words to be read	····· The number of words set by the read request is stored.
1101	Data (1)	····· Data of the set number of words are stored sequentially from the AD61C buffer memory head address set by the read request.
1102	Data (2)	

*1, *2: Data content from the head addresses of units 2 to 14 is the same.

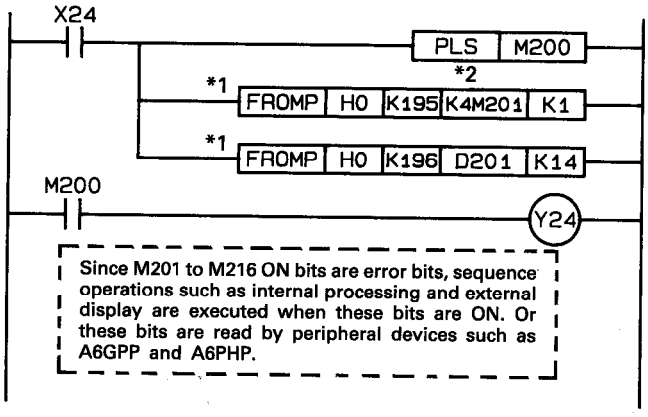
b) Read program

The read conditions are set and written to the send area. At the completion of read, receive data are read from the receive area.



*1: Since there is no FROMP instruction for the A0J2CPU (P23/R23), execute the FROM instruction by converting it a pulse instruction using an internal relay.

(4) Error detection program
MINI-S3 master module buffer memory K195 (remote terminal unit faulty station) and K196 to K209 (remote terminal unit error code) are read.



*1: Since there is no pulse instructions for the A0J2CPU (P23/R23), convert FROM instruction to pulse instruction using the internal relay.
*2: With A0J2CPU (P23/R23) and A1 to A3CPU (P21/R21), read the data to data register (D).

a) The error code which is detected by MINI-S3 master module is shown below.

Error Code (decimal)	Error Name	Error Content	Corrective Action
1	Set data error	There is an error in the data set to the AD61C send area.	Set correct data.
6	WDT error	AD61C is malfunctioning.	Confirm the AD61C LED indicators and correct following AD61C troubleshooting procedure.
8	Send area set error	AD61C send area size is insufficient.	Set the send area of the required number of bytes as send data to the AD61C.
9	Communication error	Normal communication between the master module and the AD61C cannot be executed.	• Noise ····· Execute communication again. • Check the AD61C for possible hardware error.
11			
10	Receive area set error	AD61C receive area size is insufficient.	Set the receive area of the required number of bytes as receive data from the AD61C.

b) In addition to the above error code, the error code which the AD61C detects is sent to the MINI-S3 master module and is stored in the MINI-S3 master module buffer memory. (For the AD61C error code, see Section 8.1.)

(5) Data clear processing program by AD61C reset operations and allowable communication time over

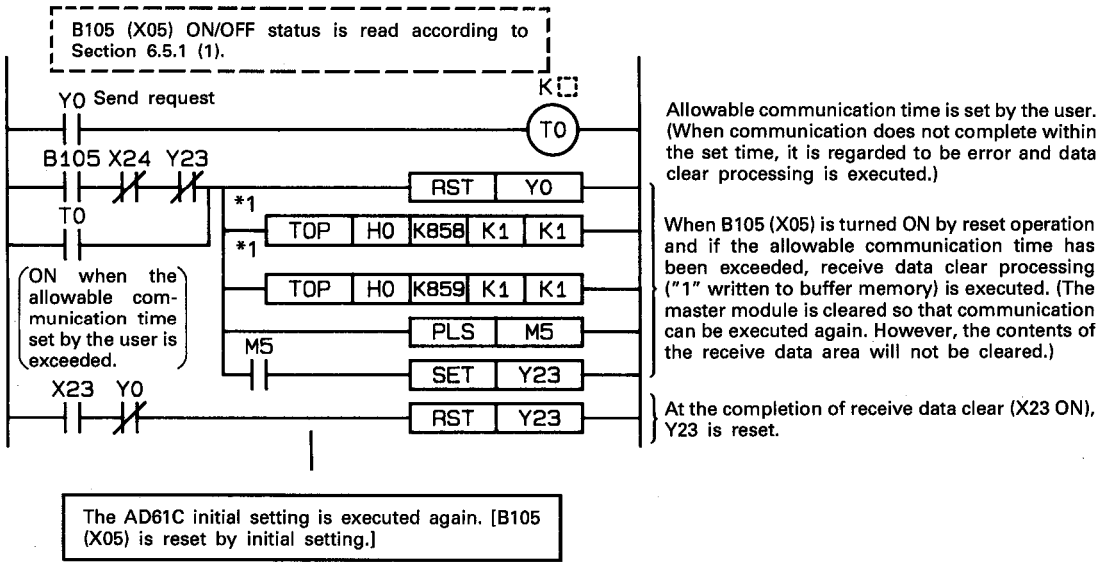
(a) When the AD61C's front reset switch is operated during communication, it is necessary to write the initial data again after detecting the reset operation and clearing the MINI-S3 master module receive data by the sequence program.

> If initial setting is not executed again after reset operations, the AD61C will not operate correctly.

(b) The detection of the AD61C reset signal is executed by the device number assigned to AD61C I/O signals.

- Reset status detection ·····X05 ON
- Reset status detection ·····Y05 ON (When Y05 is ON, is reset X05 turns OFF.)

(c) Reset signal read/write are executed according to Section 6.5.1 (1).



*1 : Since there is no pulse TO instruction for the A0J2CPU (P23/R23), execute the TO instruction after converting it into pulse instruction using an internal relay.

6.5.2 Example 1-phase/2-phase input counting programs

(1) Example counting programs for 1-phase/2-phase inputs are explained below.
- The settings for the AD61C and MINI-S3 master module are according to Section 6.5.
- CH1 is used.
- 1-phase is specified for the pulse input. (The 2-phase setting is entered in the "operation" column below.)
- Decrement count is set.
- The external coincidence signal's output is enabled.
- Preset is not executed by the external input. (Count start/stop can be executed by the external input.)
- The counter present value is not preset.
- The ring counter function is not used.

(2) The following example program is explained: I/O signal processing, initial setting, coincidence signal reset, preset, count start, coincidence processing, present value read, error detection/error code read, error code reset, receive data clear processing by reset operations.

(3) The operation items of the program order are explained in the "flow" column.

(4) The example program is explained in the "Operation" column.

(5) Initial setting values of the example program are written to the MINI-S3 master module buffer memory in batch. (These can also be written to individual addresses.)

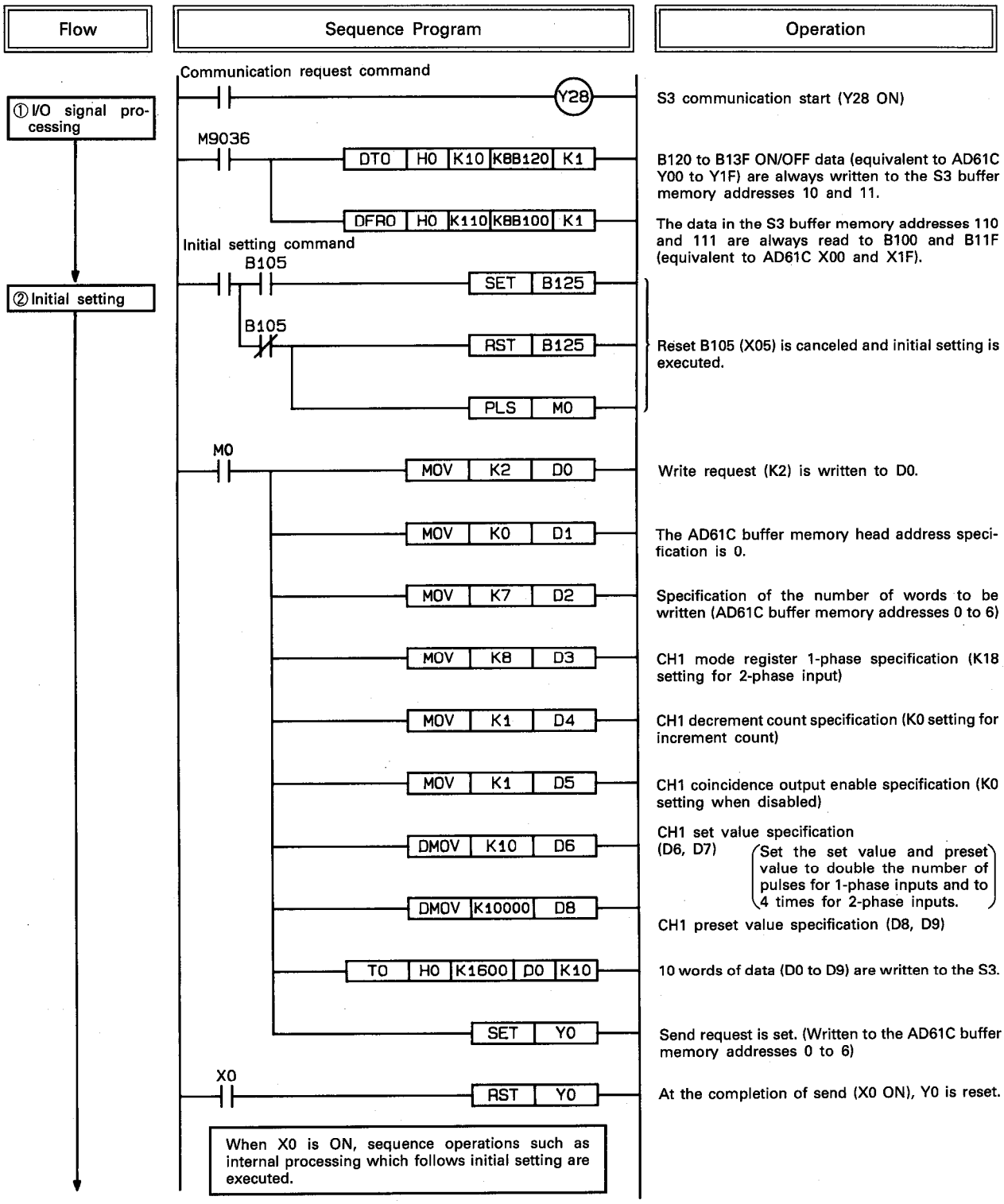
(6) I/O signals are assigned to link relay (B) as shown below.

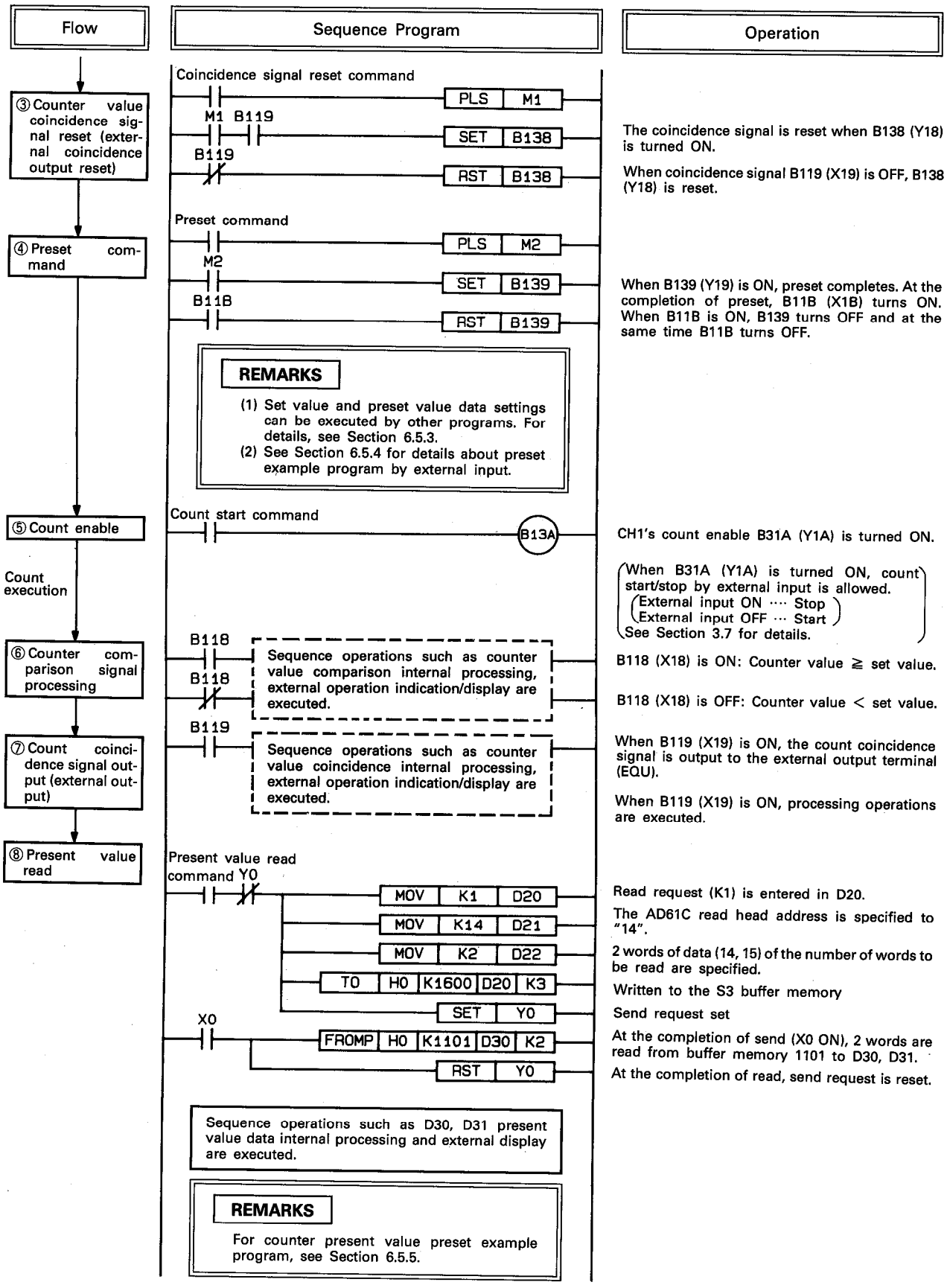
(7) Since the AD61C goes to the initial state when the ACPU or the AD61C reset switch is turned ON, execute initial setting again.

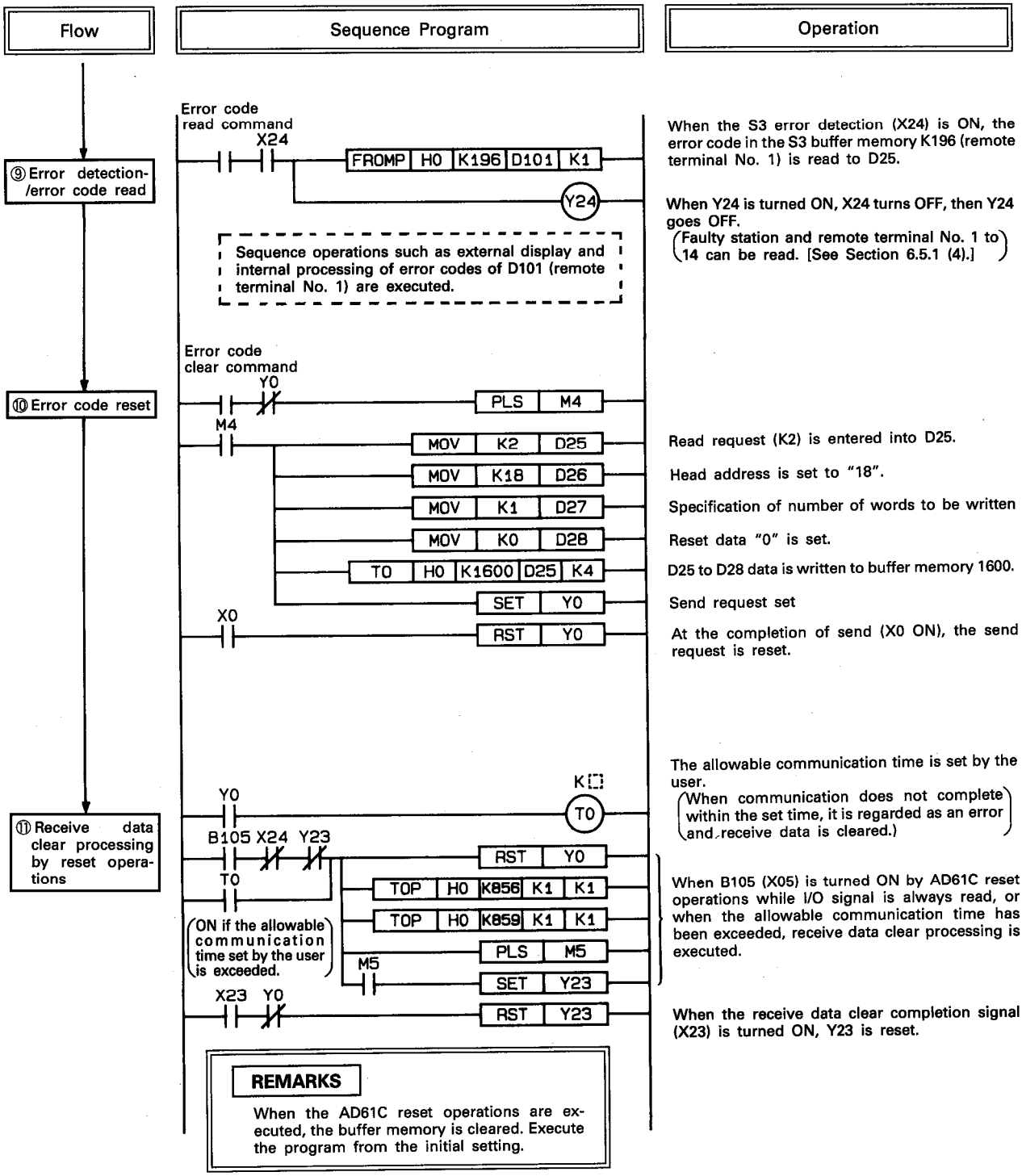
	ACPU	AD61C
Input	B100 to B10F	X00 to X0F (Uses X05)
	B110 to B11F	X10 to X1F (Uses X18 to X1F)
Output	B120 to B12F	Y00 to Y0F (Uses Y05)
	B130 to B13F	Y10 to Y1F (Uses Y18 to Y1F)

POINT

When the ACPU or the AD61C is reset, the AD61C will be reset. After resetting, be sure to execute initial setting for the AD61C.


Flow
Sequence Program
Operation
Communication request command
Y28
S3 communication start (Y28 ON)
① I/O signal processing
M9036
DTO H0 K10 K8B120 K1
B120 to B13F ON/OFF data (equivalent to AD61C Y00 to Y1F) are always written to the S3 buffer memory addresses 10 and 11.
DFRO H0 K110 K8B100 K1
The data in the S3 buffer memory addresses 110 and 111 are always read to B100 and B11F (equivalent to AD61C X00 and X1F).
Initial setting command
B105
SET B125
② Initial setting
B105
RST B125
Reset B105 (X05) is canceled and initial setting is executed.
PLS M0
M0
MOV K2 D0
Write request (K2) is written to D0.
MOV K0 D1
The AD61C buffer memory head address specification is 0.
MOV K7 D2
Specification of the number of words to be written (AD61C buffer memory addresses 0 to 6)
MOV K8 D3
CH1 mode register 1-phase specification (K18 setting for 2-phase input)
MOV K1 D4
CH1 decrement count specification (K0 setting for increment count)
MOV K1 D5
CH1 coincidence output enable specification (K0 setting when disabled)
DMOV K10 D6
CH1 set value specification (D6, D7)
Set the set value and preset value to double the number of pulses for 1-phase inputs and to 4 times for 2-phase inputs.
DMOV K10000 D8
CH1 preset value specification (D8, D9)
TO H0 K1600 D0 K10
10 words of data (D0 to D9) are written to the S3.
SET Y0
Send request is set. (Written to the AD61C buffer memory addresses 0 to 6)
X0
RST Y0
At the completion of send (X0 ON), Y0 is reset.
When X0 is ON, sequence operations such as internal processing which follows initial setting are executed.

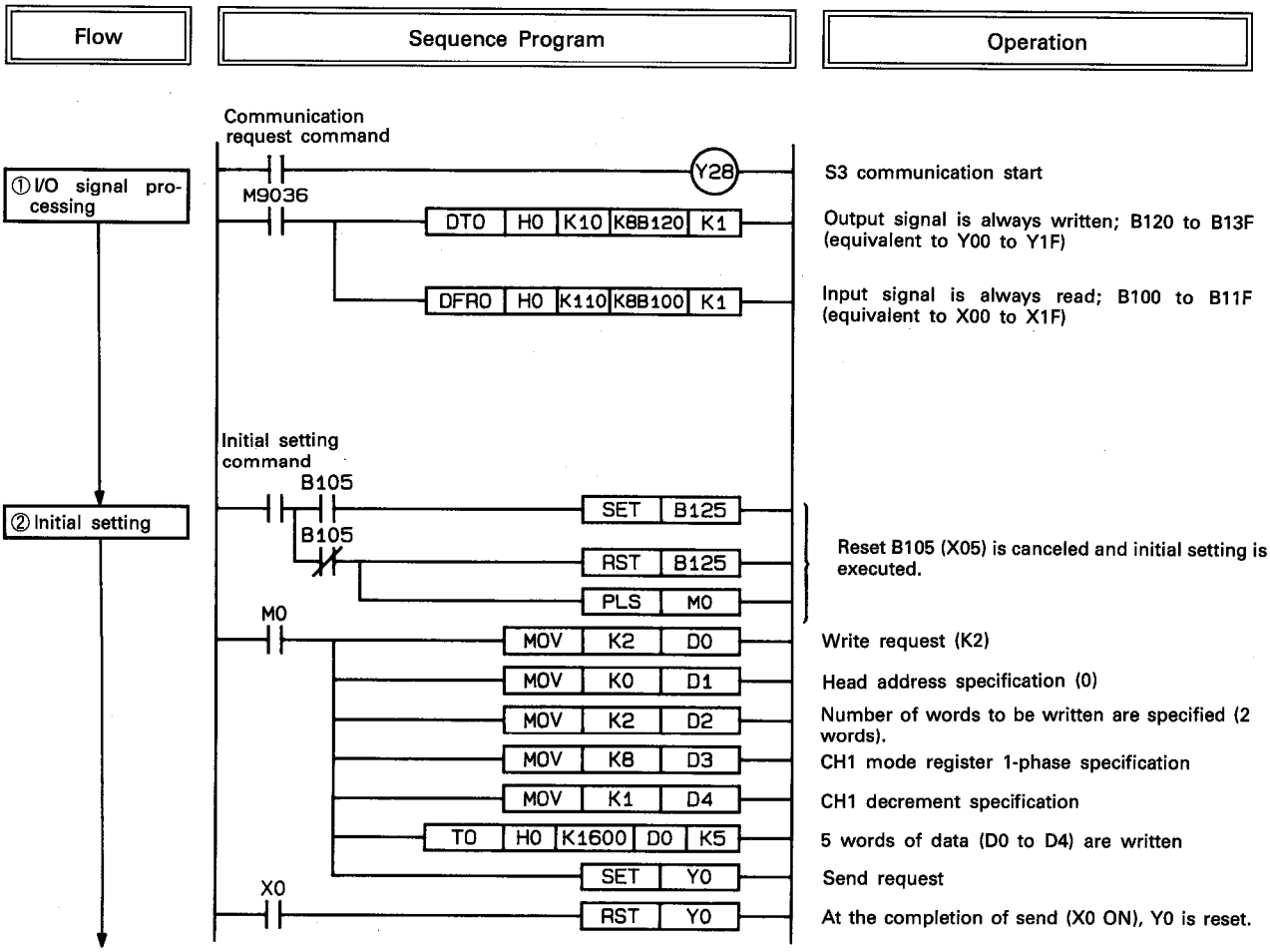

Flow
Sequence Program
Operation
③ Counter value coincidence signal reset (external coincidence output reset)
④ Preset command
⑤ Count enable
Count execution
⑥ Counter comparison signal processing
⑦ Count coincidence signal output (external output)
⑧ Present value read
Coincidence signal reset command
M1 B119
B119
PLS M1
SET B138
RST B138
The coincidence signal is reset when B138 (Y18) is turned ON.
When coincidence signal B119 (X19) is OFF, B138 (Y18) is reset.
Preset command
M2
B11B
PLS M2
SET B139
RST B139
When B139 (Y19) is ON, preset completes. At the completion of preset, B11B (X1B) turns ON. When B11B is ON, B139 turns OFF and at the same time B11B turns OFF.
REMARKS
(1) Set value and preset value data settings can be executed by other programs. For details, see Section 6.5.3.
(2) See Section 6.5.4 for details about preset example program by external input.
Count start command
B13A
CH1's count enable B31A (Y1A) is turned ON.
When B31A (Y1A) is turned ON, count start/stop by external input is allowed.
External input ON ···· Stop
External input OFF ··· Start
See Section 3.7 for details.
B118
B118
Sequence operations such as counter value comparison internal processing, external operation indication/display are executed.
B118 (X18) is ON: Counter value ≧ set value.
B118 (X18) is OFF: Counter value < set value.
B119
Sequence operations such as counter value coincidence internal processing, external operation indication/display are executed.
When B119 (X19) is ON, the count coincidence signal is output to the external output terminal (EQU).
When B119 (X19) is ON, processing operations are executed.
Present value read command Y0
MOV K1 D20
MOV K14 D21
MOV K2 D22
TO H0 K1600 D20 K3
SET Y0
X0
FROMP H0 K1101 D30 K2
RST Y0
Read request (K1) is entered in D20.
The AD61C read head address is specified to "14".
2 words of data (14, 15) of the number of words to be read are specified.
Written to the S3 buffer memory
Send request set
At the completion of send (X0 ON), 2 words are read from buffer memory 1101 to D30, D31.
At the completion of read, send request is reset.
Sequence operations such as D30, D31 present value data internal processing and external display are executed.
REMARKS
For counter present value preset example program, see Section 6.5.5.

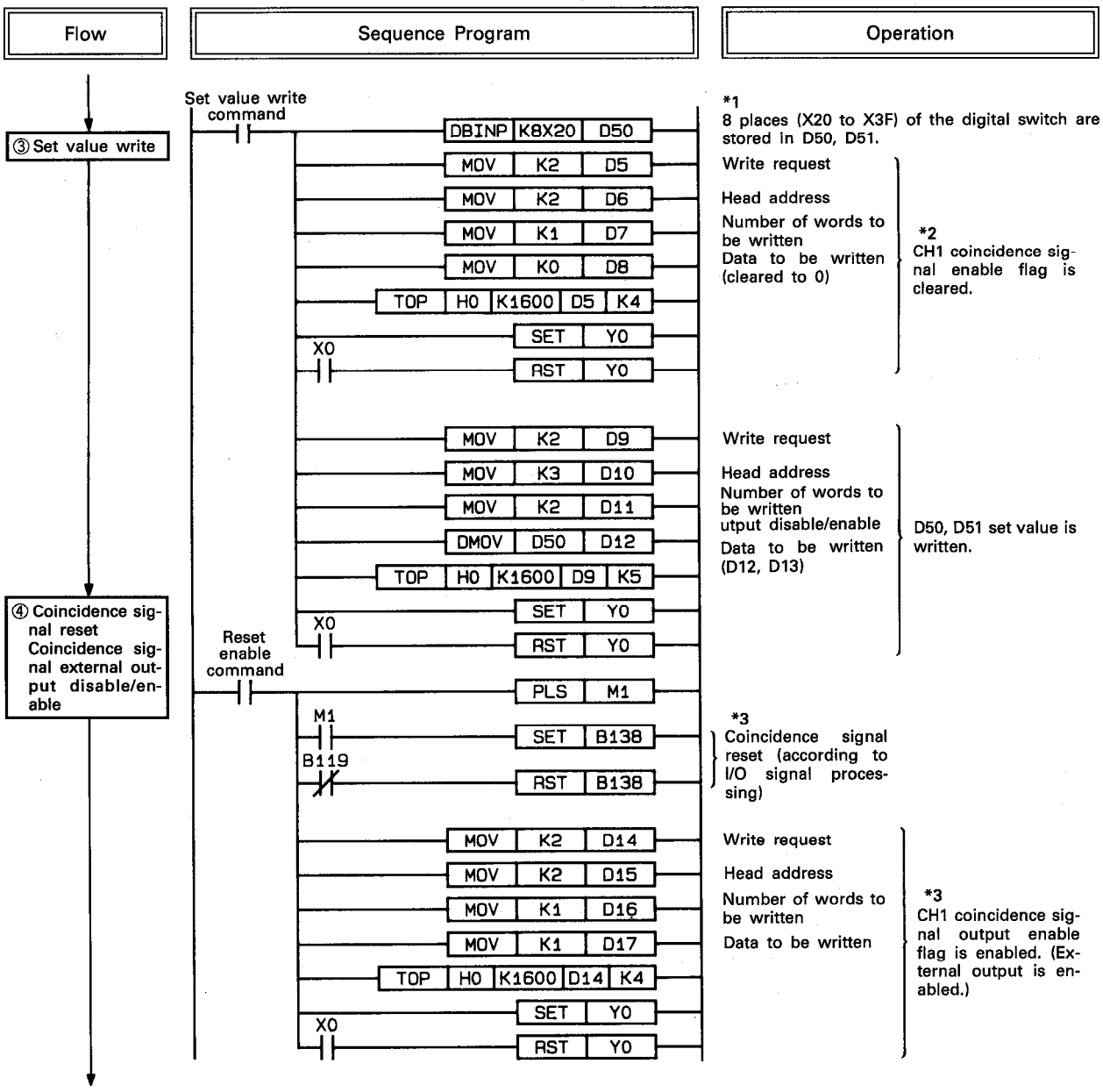

Flow
Sequence Program
Operation
⑨ Error detection-/error code read
⑩ Error code reset
⑪ Receive data clear processing by reset operations
Error code read command
X24
FROMP H0 K196 D101 K1
Y24
When the S3 error detection (X24) is ON, the error code in the S3 buffer memory K196 (remote terminal No. 1) is read to D25.
When Y24 is turned ON, X24 turns OFF, then Y24 goes OFF.
(Faulty station and remote terminal No. 1 to 14 can be read. [See Section 6.5.1 (4).])
Sequence operations such as external display and internal processing of error codes of D101 (remote terminal No. 1) are executed.
Error code clear command
Y0
PLS M4
M4
MOV K2 D25
Read request (K2) is entered into D25.
MOV K18 D26
Head address is set to "18".
MOV K1 D27
Specification of number of words to be written
MOV K0 D28
Reset data "0" is set.
T0 H0 K1600 D25 K4
D25 to D28 data is written to buffer memory 1600.
SET Y0
Send request set
X0
RST Y0
At the completion of send (X0 ON), the send request is reset.
K□
Y0
T0
The allowable communication time is set by the user.
(When communication does not complete within the set time, it is regarded as an error and receive data is cleared.)
B105 X24 Y23
RST Y0
T0
TOP H0 K856 K1 K1
TOP H0 K859 K1 K1
PLS M5
M5
SET Y23
(ON if the allowable communication time set by the user is exceeded.)
When B105 (X05) is turned ON by AD61C reset operations while I/O signal is always read, or when the allowable communication time has been exceeded, receive data clear processing is executed.
X23 Y0
RST Y23
When the receive data clear completion signal (X23) is turned ON, Y23 is reset.
REMARKS
When the AD61C reset operations are executed, the buffer memory is cleared. Execute the program from the initial setting.

6.5.3 Example program for setting set value and preset value data

Based on the example sequence program of Section 6.5.2, the example program in which the set value and preset value are fetched by the external digital switch and written to the AD61C is shown.

The necessary program is obtained by replacing sequences from [(1) initial setting] to [(4) preset command] of Section 6.5.2 with the following sequences.

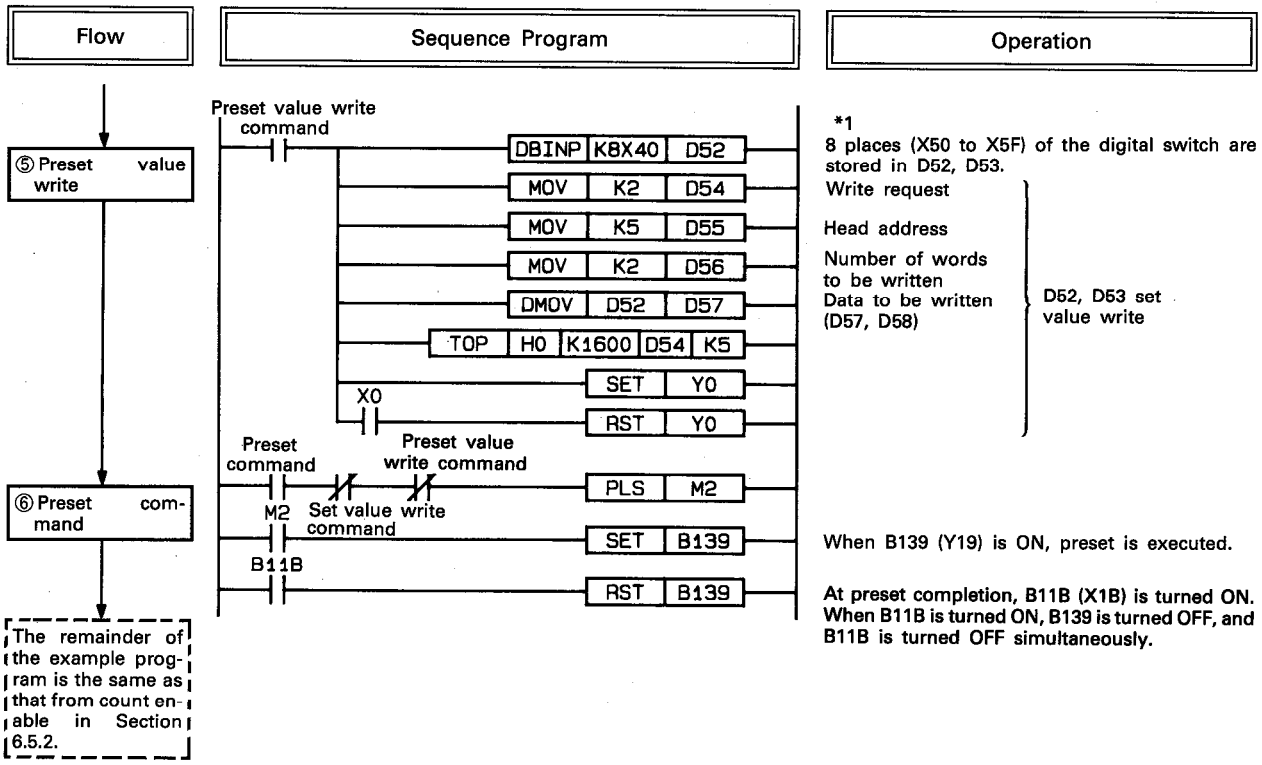




*1 : Set the set value and preset value to double the number of pulses for 1-phase inputs and to 4 times for 2-phase inputs.

*2 : Clear the coincidence signal output enable flag before writing set value. (The counter value and set value might coincide when set value data is being written and therefore the coincidence signal should not be output externally.)

*3 : Execute coincidence signal reset after set value write and set the coincidence signal output enable flag.



*1 : Set the set value and preset value to double the number of pulses for 1-phase inputs and to 4 times for 2-phase inputs.

6.5.4 Example preset program by external input

Based on the example sequence programs of Sections 6.5.2 and 6.5.3, an example program in which the preset command is executed from the external input terminal (PRST terminal) is shown below.

An example program is obtained by replacing (3) preset command program of Section 6.5.2 and (4) preset command program of Section 6.5.3 with the following sequences.

Flow	Sequence Program	Operation
① Preset command (external input)	External preset request detection reset instruction B11A B11B — SET B13B B11A — RST B13B	When external preset request detection [B11A (X1A)] and preset complete [B11B (X1B)] by external input are ON, CH1 external preset request detection reset [B31B (Y1B)] is turned ON and the external preset request detection signal [B11A (X1A)] is reset: When B11A (X1A) is turned OFF, B31B (Y1B) is reset.

CAUTION

(1) In preset operations by external input, if the preset signal is input to the external terminal (PRST terminal), the external preset request detection B11A (X1A) is turned ON at the preset input's rising edge and the buffer memory internal preset value is preset to the counter value. (See Section 3.4 for details.)

(2) When presetting by external input, reset the external preset request detection each time preset is completed. The next external input is allowed after the external preset request detection is reset.

(3) If the external preset request detection B11A (X1A) is ON, preset by external input and preset command B139 (Y19) by the sequence program cannot operate.

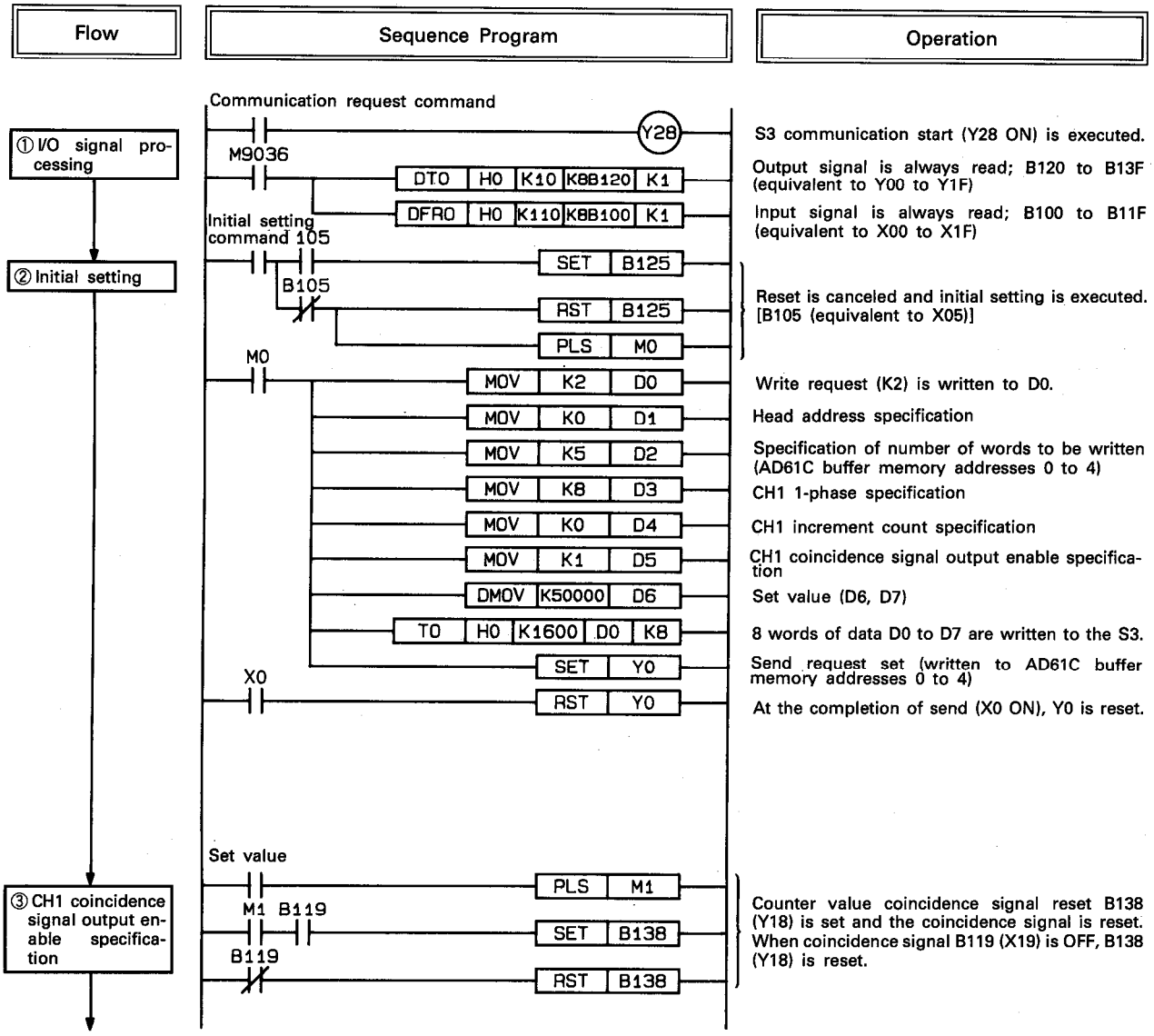
(4) If preset by external input terminal (PRST terminal) is not to be executed, execution of the above program is not necessary.

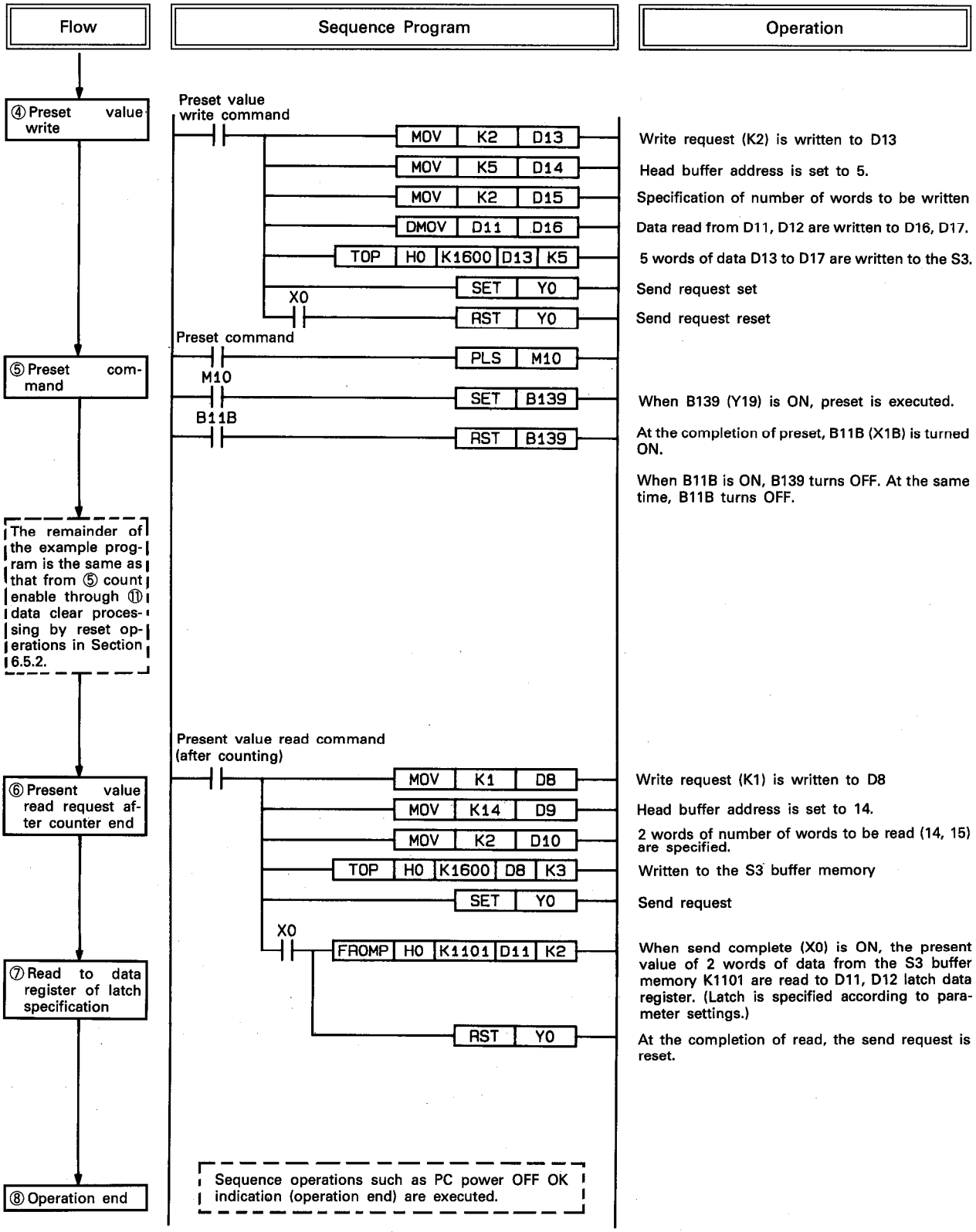
6.5.5 Example program of counter present value preset

An example program in which the counter present value, before the ACPU is turned OFF or at count end, is read and counting continues by presetting the read present value before starting the next counting is shown below.

This example program is explained according to the following conditions.

- AD61C station number is set to "01" (occupying stations Nos. 1 to 4) and remote terminal number is set to "1".
- CH1 is used.
- 1-phase is specified for the pulse input.
- Increment count is specified.
- The external coincidence signal output is enabled.
- The total number of pulses for the set value is 50,000 (25,000 × 2). The first preset value is 0 (default value).
- The ring counter function is not used.



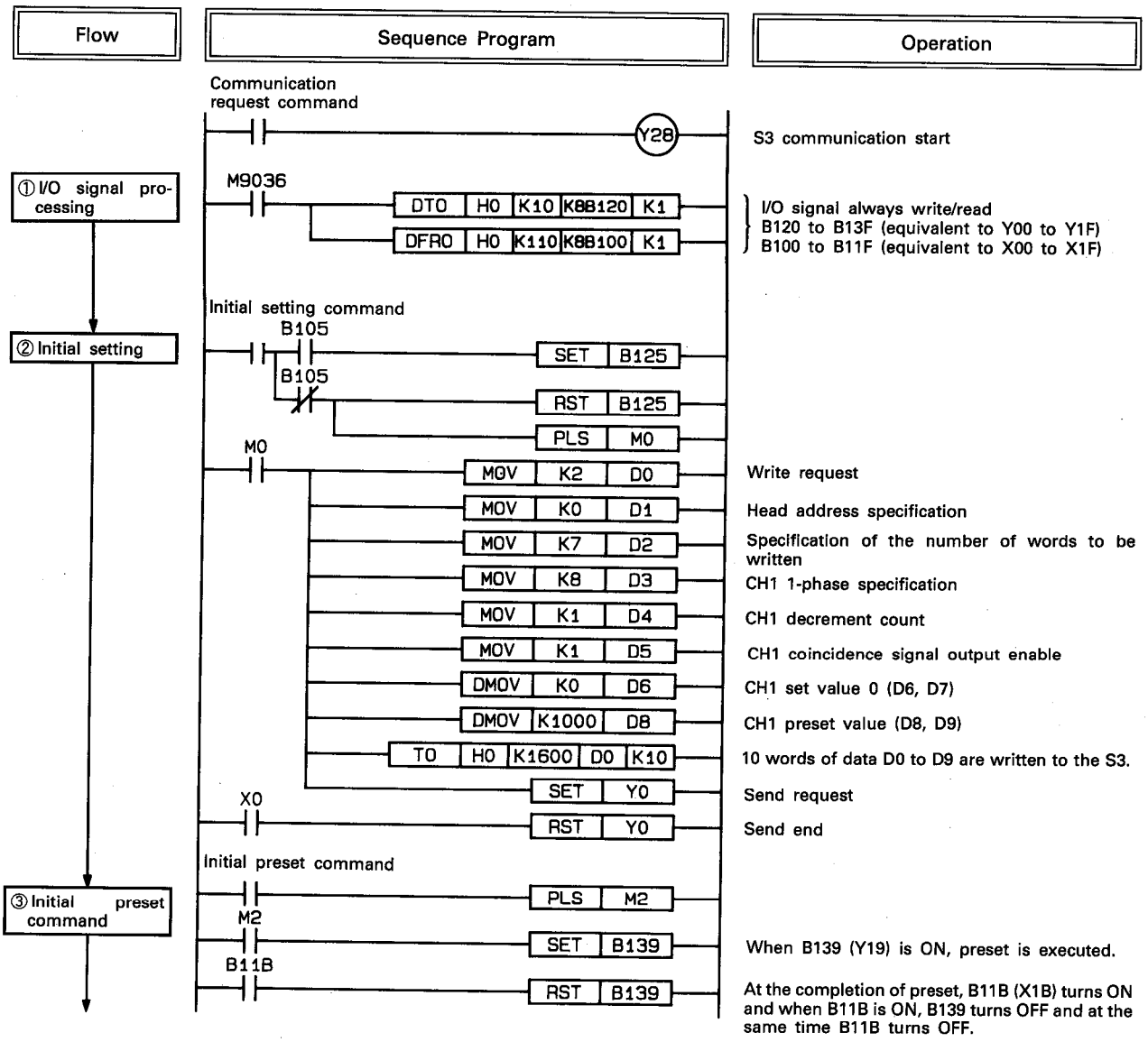

Flow
Sequence Program
Operation
④ Preset value write
Preset value write command
MOV K2 D13
Write request (K2) is written to D13
MOV K5 D14
Head buffer address is set to 5.
MOV K2 D15
Specification of number of words to be written
DMOV D11 D16
Data read from D11, D12 are written to D16, D17.
TOP H0 K1600 D13 K5
5 words of data D13 to D17 are written to the S3.
SET Y0
Send request set
X0
RST Y0
Send request reset
Preset command
⑤ Preset command
PLS M10
M10
SET B139
When B139 (Y19) is ON, preset is executed.
B11B
RST B139
At the completion of preset, B11B (X1B) is turned ON.
When B11B is ON, B139 turns OFF. At the same time, B11B turns OFF.
The remainder of the example program is the same as that from ⑤ count enable through ⑪ data clear processing by reset operations in Section 6.5.2.
Present value read command (after counting)
⑥ Present value read request after counter end
MOV K1 D8
Write request (K1) is written to D8
MOV K14 D9
Head buffer address is set to 14.
MOV K2 D10
2 words of number of words to be read (14, 15) are specified.
TOP H0 K1600 D8 K3
Written to the S3 buffer memory
SET Y0
Send request
X0
⑦ Read to data register of latch specification
FROMP H0 K1101 D11 K2
When send complete (X0) is ON, the present value of 2 words of data from the S3 buffer memory K1101 are read to D11, D12 latch data register. (Latch is specified according to parameter settings.)
RST Y0
At the completion of read, the send request is reset.
⑧ Operation end
Sequence operations such as PC power OFF OK indication (operation end) are executed.

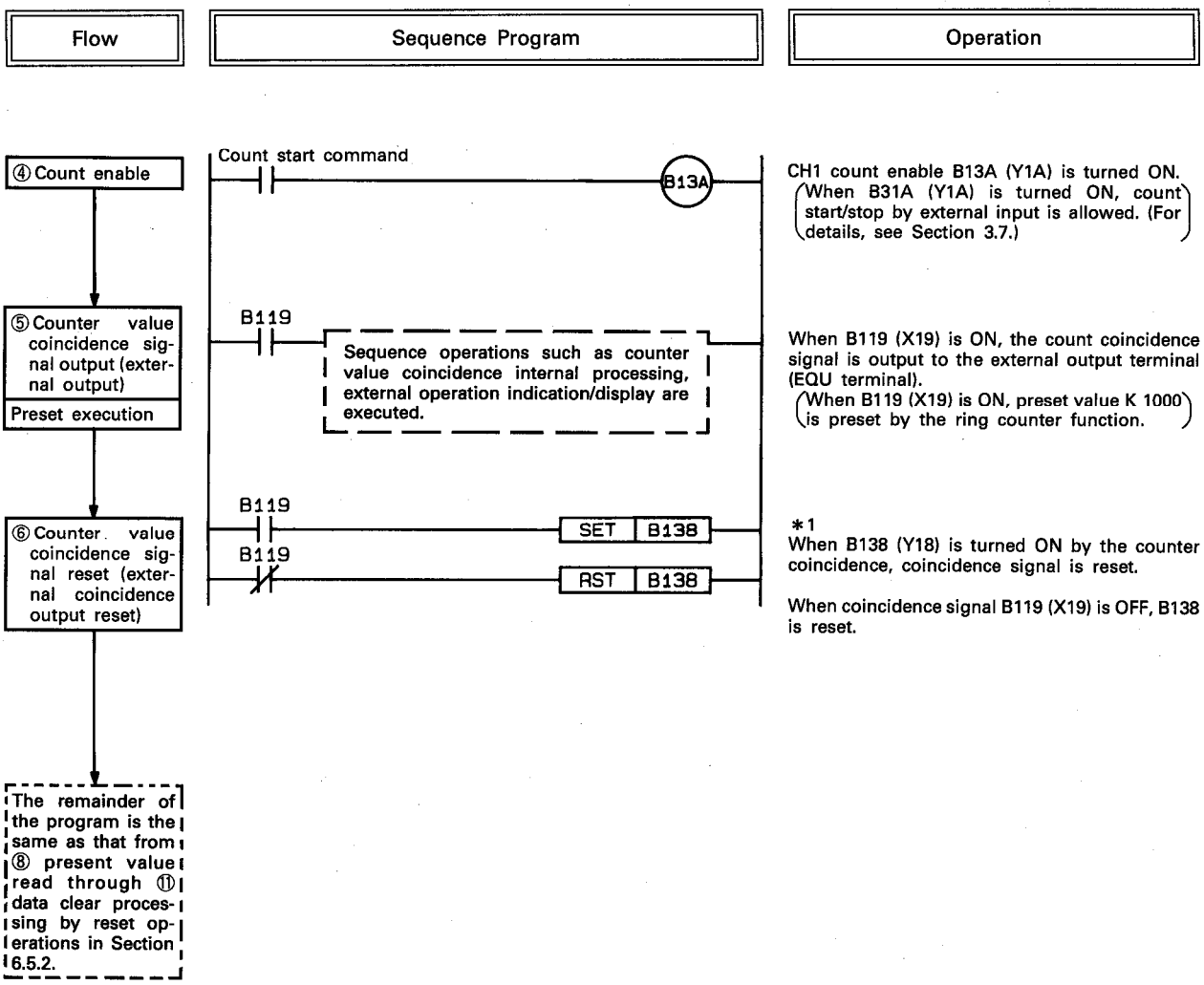
6.5.6 Example program of ring counter function

An example program in which ring count is executed by turning ON the ring counter switch is shown below.

This example program is explained according to the following conditions.

- AD61C station number is set to "01" (occupying stations Nos. 1 to 4) and remote terminal number is set to "1".
- CH1 of the AD61C ring counter setting switch is turned ON.
- Only CH1 buffer memory is used and 1-phase is specified for the pulse input.
- Decrement count is specified.
- The external coincidence signal output is enabled.
- Preset is not executed by the external input.
- Count start/stop can be executed by the external input.
- The set value is 0 and the number of pulses for the preset value is 1000 (500 × 2).





*1 : When using the ring counter function, be sure to reset counter coincidence signal B119 (X19). If B119 (X19) is left ON, the next preset cannot be executed.

6.5.7 Programs when 2 channels are used

Programs using 2 channels are explained.

(1) A CH2 example program is created in the same way as CH1 example programs in Sections 6.5.2 to 6.5.6.

(2) The execution content program of CH2 is added as indicated below following the order of the example program Flow.

(3) Regarding FROM/TO instructions to be executed for buffer memory, read/write is possible in batch in the range which the buffer memory can be specified. (See REMARKS)

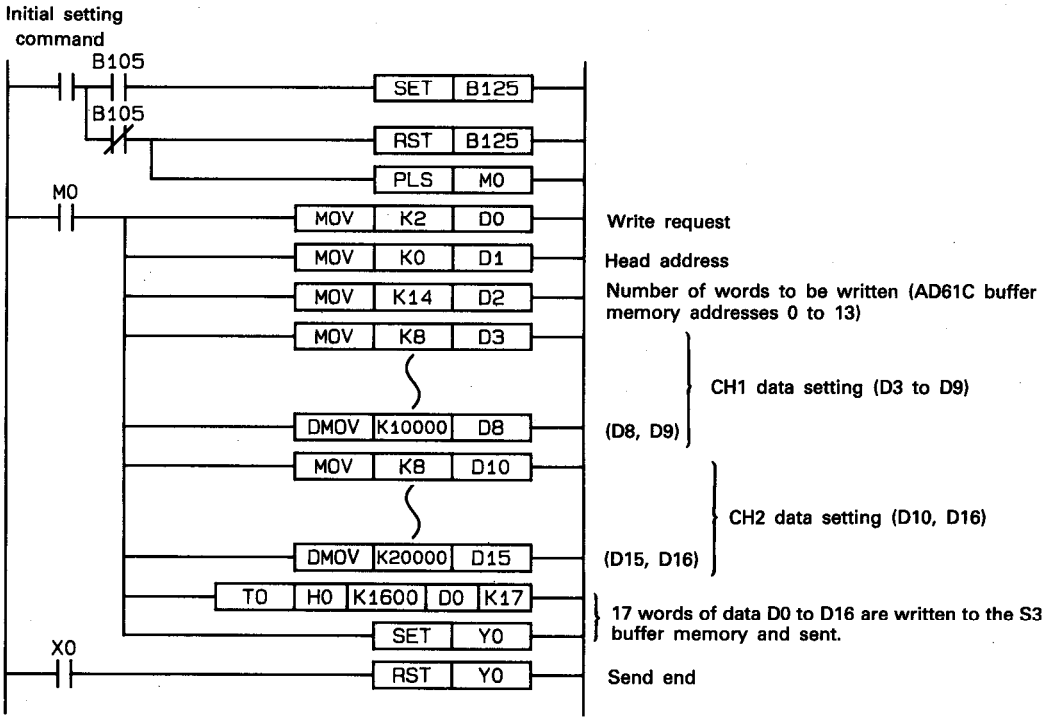
(4) FROM/TO instructions can be used for each buffer memory address.

(5) See Sections 6.3 and 6.4 regarding CH2 I/O signals and buffer memory addresses.

(6) For I/O signal processing in the example program, CH1 and CH2 are treated simultaneously. Therefore, create programs using CH2 I/O signals.

REMARKS

- The program which writes CH1 and CH2 initial settings in batch is shown below.

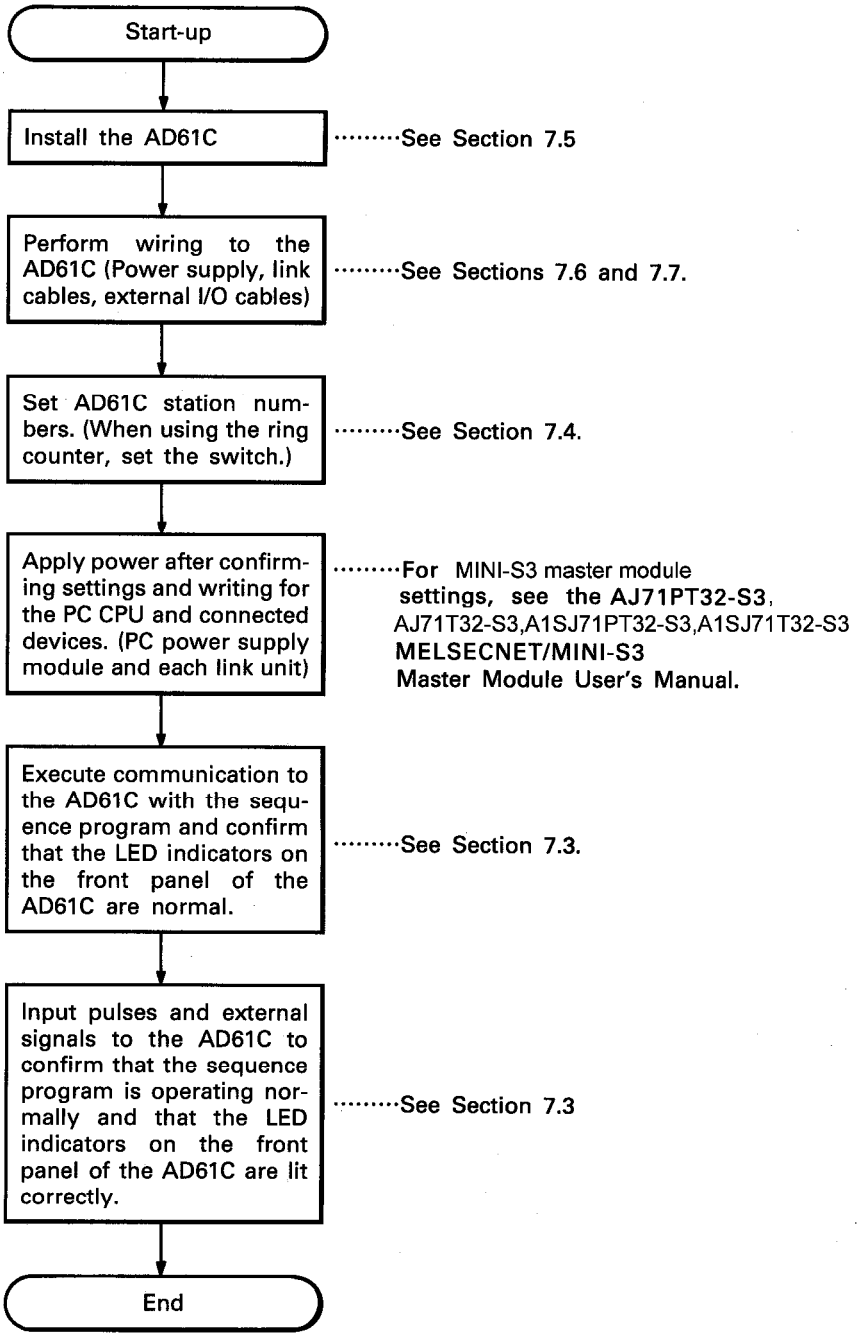


7. INSTALLATION AND PRE-OPERATION SETTING PROCEDURES

Pre-operation procedures for the AD61C, the names and settings for each part of the AD61C, and the wiring method are explained in this section.

7.1 Pre-operation Setting Procedures

Pre-operation setting procedures for the AD61C are explained below.



7.2 Handling Precautions

Handling precautions for the AD61C are explained below.

(1) The case is aluminum diecast. However, since the LED display is made of resin and the printed circuit board is embedded in the case, protect it from impact.

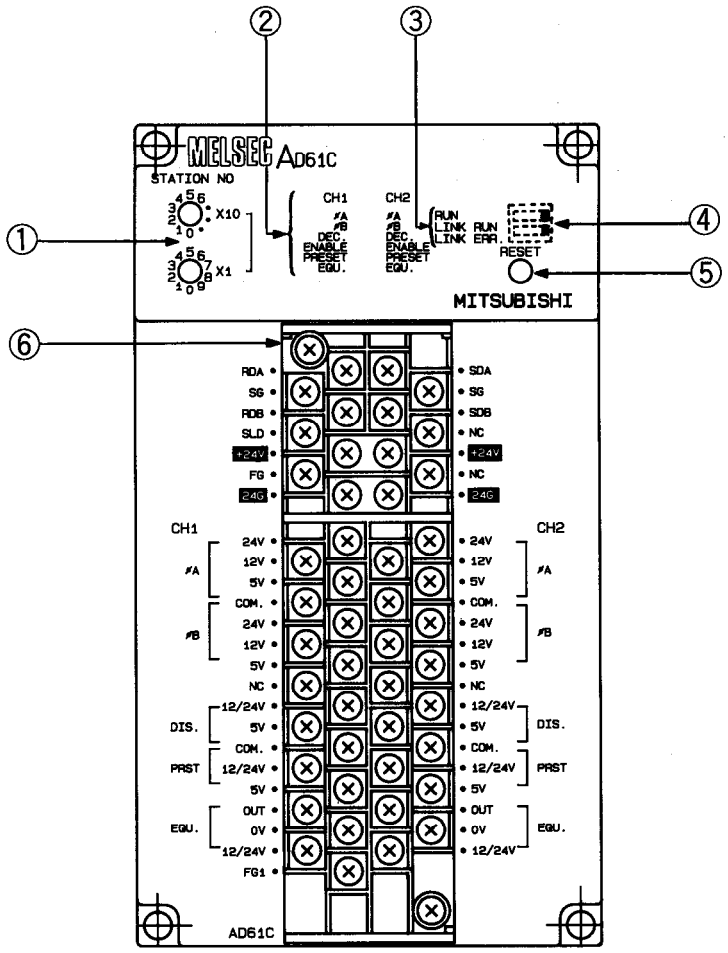
(2) Do not remove the printed circuit board from the case.

(3) When wiring, be sure that no wire offcuts remain around the terminal block.

(4) Tighten the terminal block's terminal screws (M3.5 screw) within a tightening torque range 68.6 to 98 (N · cm).

(5) Tighten the AD61C's installation screws (M4 screw) within a tightening torque range of 78.5 to 118.7 (N · cm).

7.3 Nomenclature



<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>①</td><td>Station number setting switch</td><td>• Sets the station number from 01 to 61 by rotary switch.
• Station 00 is a bypass function. (For details, see Section 7.4.1.)</td></tr>
<tr><td>②</td><td>CH1, CH2 operating status indication LED</td><td>LEDs for operating status indication
<table>
<tr><th>LED</th><th>Confirmation</th></tr>
<tr><td>φA (phase A pulse input indication)</td><td>Lit when voltage is applied to phase A pulse input terminal</td></tr>
<tr><td>φB (phase B pulse input indication)</td><td>Lit when voltage is applied to phase B pulse input terminal</td></tr>
<tr><td>DEC (operation in progress indication)</td><td>• Lit at 1-phase decrement specification
• Lit at 2-phase decrement specification</td></tr>
<tr><td>ENABLE (count input enable)</td><td>• Lit when disable input is OFF and count enable is ON</td></tr>
<tr><td>PRESET (external preset input detection)</td><td>• Lit and latched when voltage is applied to preset input terminal
• OFF when external preset detection reset signal is ON</td></tr>
<tr><td>EQU (external coincidence output operation in progress)</td><td>• Lit when the counter value coincidence signal and the external output enable are ON</td></tr>
</table></td></tr>
<tr><td>③</td><td>Operation state indicator LED</td><td>LEDs for operating status, and error definition indication, etc.
<table>
<tr><th>LED</th><th>Confirmation</th></tr>
<tr><td>RUN</td><td>• ON: Normally running
• Flicker: Write data error*1
• OFF: 24 VDC is off or WDT error*1</td></tr>
<tr><td>LINK RUN</td><td>• ON: Link is normal
• OFF: Link error is detected at power on.*1</td></tr>
<tr><td>LINK ERR.</td><td>• ON: Error is detected during link.*1
• OFF: Link is normal</td></tr>
</table>
*1 : For error details, see Sections 8.2 to 8.4.</td></tr>
<tr><td>④</td><td>Ring counter setting switch</td><td>Switch for setting ring counter function (For details, see Section 7.4.2.)</td></tr>
<tr><td>⑤</td><td>Reset switch</td><td>AD61C hardware reset (initialization) switch</td></tr>
<tr><td>⑥</td><td>I/O terminal block</td><td>• Terminal block for data link cable wiring, 24 V power supply wiring, CH1, CH2 I/O wiring. (For wiring details, see Sections 7.6 and 7.7.)</td></tr>
</table>

7.4 Settings

7.4.1 Station number settings

(1) Settings for the AD61C station number setting switches are explained below.

	Setting
×10 ×1	(1) Switch of x 10 : Set 2nd digit of station number (2) Switch of x 1 : Set 1st digit of station number (3) Set station numbers in the range of 01 to 61. (4 stations/module) (4) Set station number 00 as a bypass function (relay).

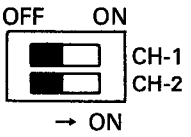
(2) This switch number is set to "00" at shipment.

(3) For precautions about station number settings when connected to MELSECNET/MINI-S3, see the manuals below.

- A2CCPU (P21-R21), A2CCPU-DC24V, A2CCPUC24(-PRF),A2CJCPU User's Manual
- AJ71PT32-S3,AJ71T32-S3,A1SJ71PT32-S3,A1SJ71T32-S3 MELSECNET/MINI-S3 master module User's Manual

7.4.2 Ring counter settings

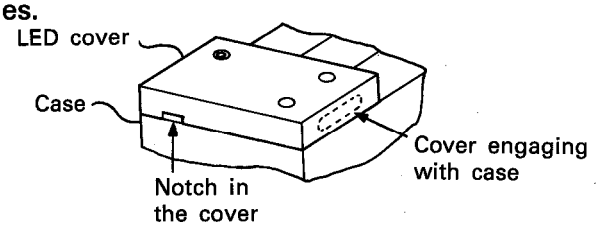
(1) Setting of the AD61C ring counter setting switch is explained below.

	Setting
	(1) Remove the LED cover. (2) Slide the switch in the ON position for the channel which uses the ring counter function. (3) Install the LED cover.

(2) This switch is set to OFF at shipment.

(3) The LED cover is removed and installed as follows.

1) Holding the LED cover, pull the case at the sides. If it does not readily detach, insert a regular screwdriver into the notch in the cover and pry it to detach the cover.
2) To install, insert the cover horizontally while pressing the top of its sides.



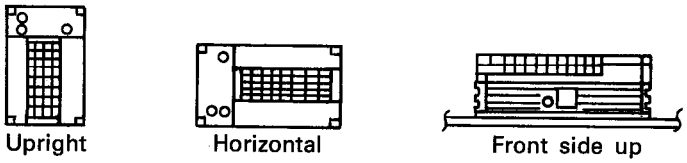
7.5 Mounting Procedures

This section gives mounting procedures of the AD61C including mounting directions and use of the DIN rail adapter.

7.5.1 Mounting directions

(1) The AD61C can be mounted in any direction (Front side must not face downward.)

(2) Examples



7.5.2 DIN rail adapter

This section describes specifications and handling instructions of the DIN rail adapter.

(1) Type · dimensions · weight

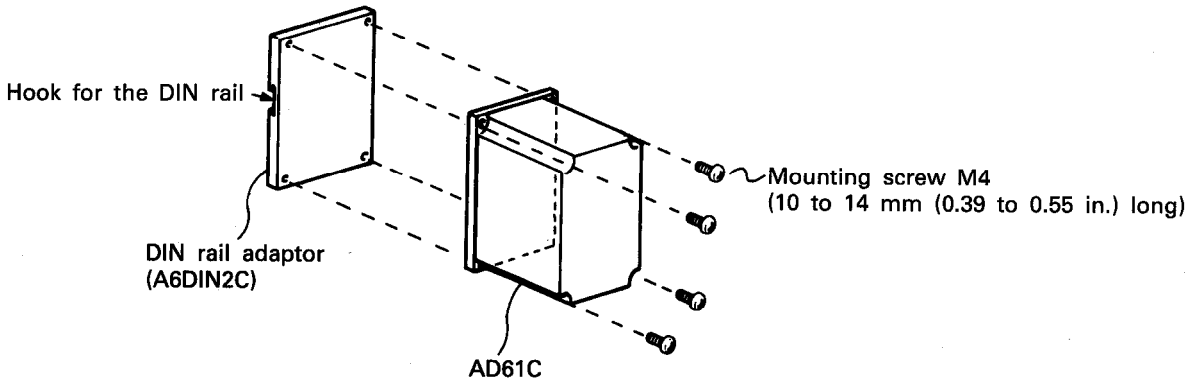
Type	A6DIN2C
Dimensions	172 (6.77) × 104 (4.09) × 10 mm (0.39 in)
Weight	0.1kg

(2) Handling instructions

1) Do not drop or give hard shocks to the DIN rail adapter since it is made of plastic.

2) Use 4 M4 screws of 10 mm to 14 mm (0.55 in. to 0.39 in.) long to fix a DIN rail adapter to a module. Torque range should be 78.5 to 118.7N · cm.

(3) Fixing to the AD61C module



7.5.3 Mounting to the DIN rail

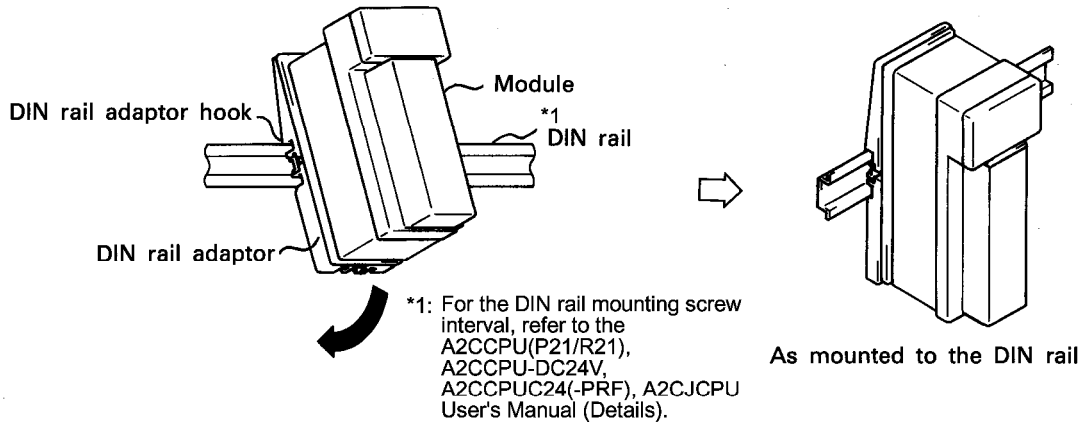
Installation to and removal from the DIN rail is explained below.

(1) Mounting procedure

After fixing the DIN rail adapter to the module, mount the module to the DIN rail as follows.

(a) Engage the hook of the adapter with the rail from above the rail.

(b) Push the module onto the rail and fix it in position.



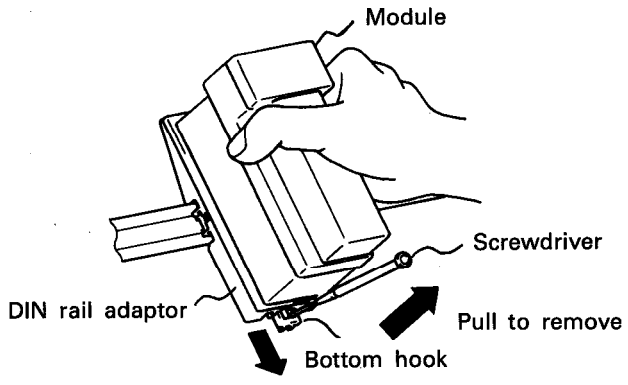
(c) When two adapters with module are mounted to the rail side by side without leaving a clearance between them, a 4 mm (0.16 in.) clearance is allowed between the modules. (See Appendix 2. External Dimensions for dimensions of the DIN adapter.)

(2) Removing procedure

Remove the module from the DIN rail as follows.

(a) Pull down the bottom hook of the adapter using a screwdriver.

(b) Pull the module away from the rail while pulling down the bottom hook.



7.6 Wiring of Data Link Cables

7.6.1 Handling instructions for twisted pair cables

Handle cables with special care.

(1) Do not compress the cable with rigid and sharp-edged material.

(2) Do not twist the cable extremely.

(3) Do not tense strong the cable.

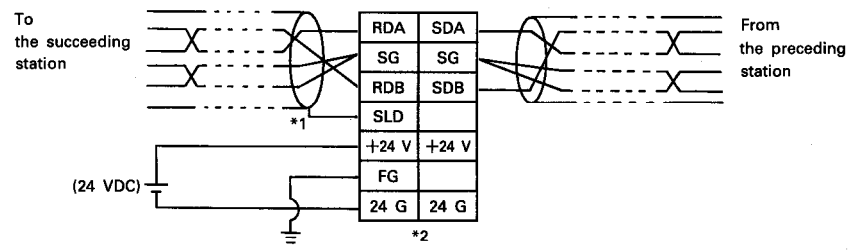
(4) Do not step on the cable

(5) Do not put things on the cable.

(6) Do not damage the insulation of the cable.

7.6.2 Link cable connections

Twisted pair cables are connected as shown below.



*1: Wire the shield to the SLD terminal.

*2: Terminal screws are M3.5 screws. Use solderless terminals matching terminal screws.

POINT

Twisted pair cables must be connected so that they may not be influenced by noise or serge induction.

(1) Do not lay the cables close to nor bind them together with main circuit wires, high-tension wires or load carrying wires. (allow 100 mm (3.94 in.) or more clearance)

(2) When connecting to the remote module terminal block, allow maximum clearance between twisted pair cables and module power supply lines and I/O signal wires.

(3) Do not use a part of twisted pair cables (such as one pair among 3 pairs) for power supply.

7.7 Connecting External Devices

7.7.1 Wiring instructions

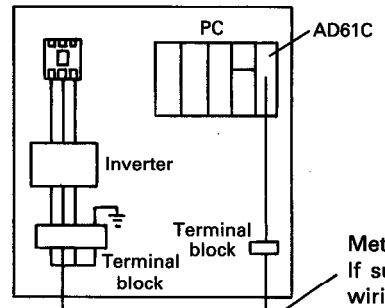
(1) When using high speed pulse inputs, take the following precautions against noise in wiring.

a) Be sure to use shielded twisted pair cables. Also provide Class 3 grounding.

b) Do not run a twisted pair cable in parallel with power cables or other I/O lines which may generate noise. Run cables at least 150 mm (5.91 in.) away from the above described lines and over the shortest distance possible.

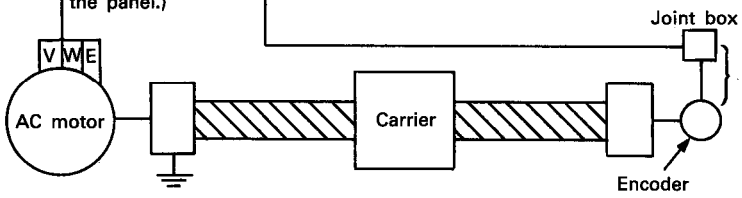
(2) For 1-phase input, connect count input signal only to phase A; for 2-phase input, connect to phases A and B.

(3) If the AD61C picks up pulse noises, it will miscount. Noise precautions are shown below.

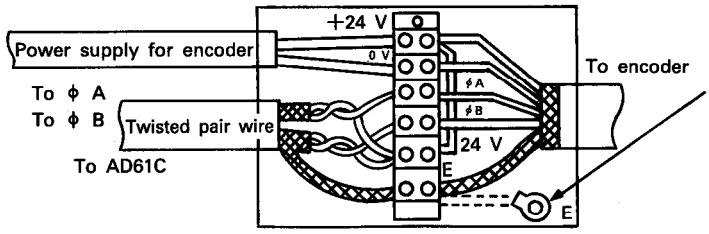


Metal piping. Never run solenoid or inductive wiring through the same conduit. If sufficient distance cannot be provided between the high current line and input wiring, use shielded wire for the high current line.

Separate more than 150 mm from equipment such as inverters, etc. (Also take care of wiring inside the panel.)



Distance between encoder and joint box should be as short as possible.If the distance from the AD61C to the encoder is too long an excessive voltage drop occurs. Therefore, measure the voltage during operation and check that the voltages are within the rated voltage of the encoder. If the voltage drop is large, increase the size of wiring or use as encoder of 24 VDC with less current consumption.



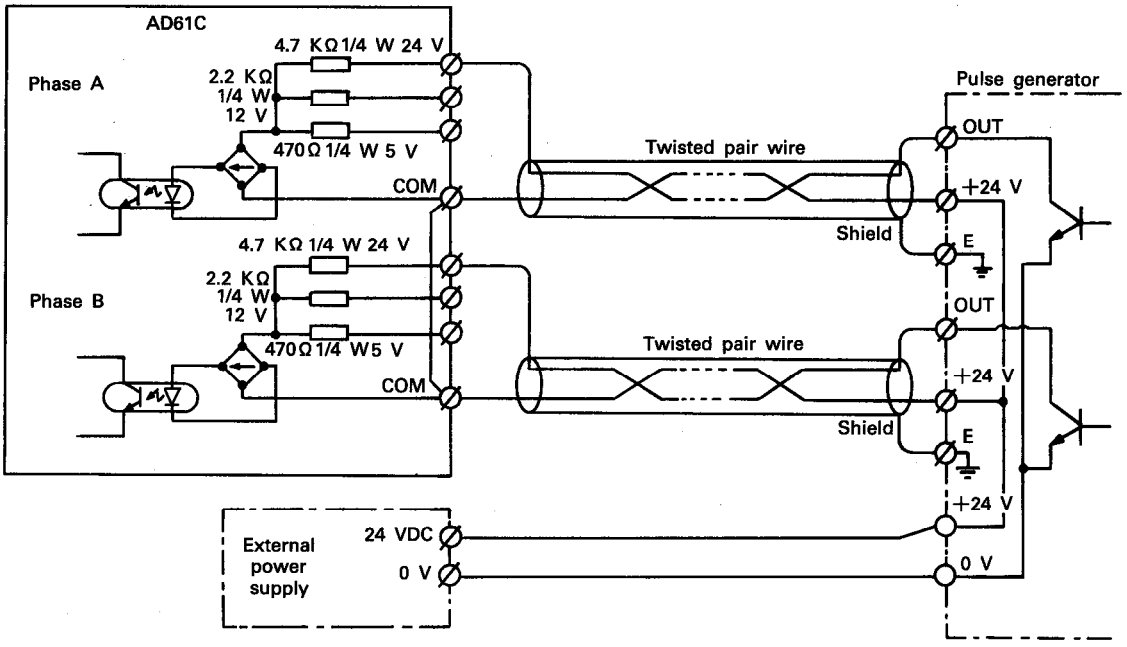
Ground twisted shield wire on the encoder side (joint box).
(This is a connection example for 24 V send load.)
Connect the encoder shield wire to the twisted pair shield wire inside the joint box. If the shield wire of the encoder is not grounded in the encoder, ground it inside the joint box as indicated by dotted line.

POINT

Before applying power to the pulse generator, confirm that the power supply matches the voltage indication levels of phase A and B input terminals. Applying 24 V to a 5 V terminal will cause damage to pulse generator.

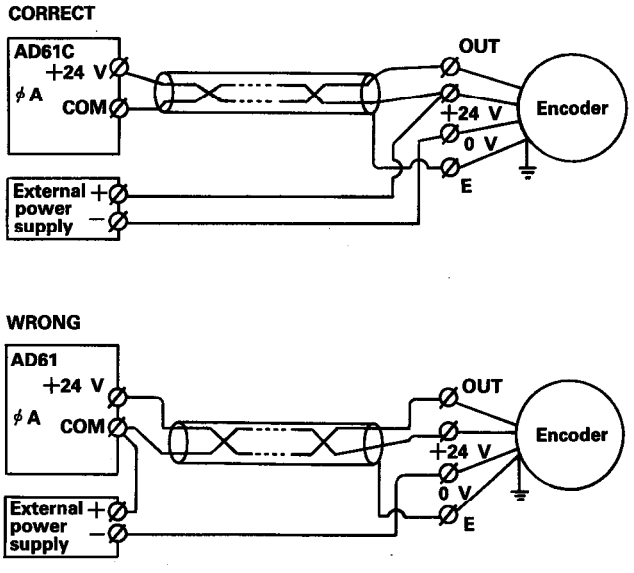
7.7.2 Wiring example for the connection with the open collector output pulse generator

(1) Connection of a 24 VDC pulse generator



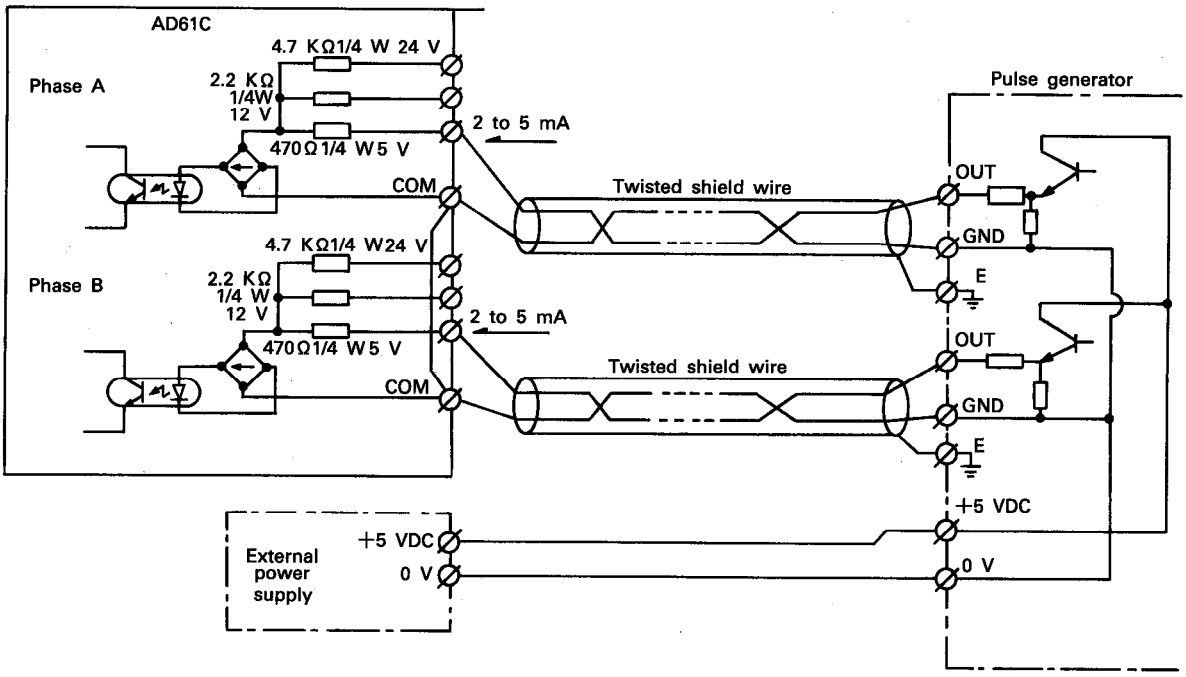
POINT

In order to minimize any interference from noise on the encoder power supply, the encoder signal and supply lines should be wired as follows:



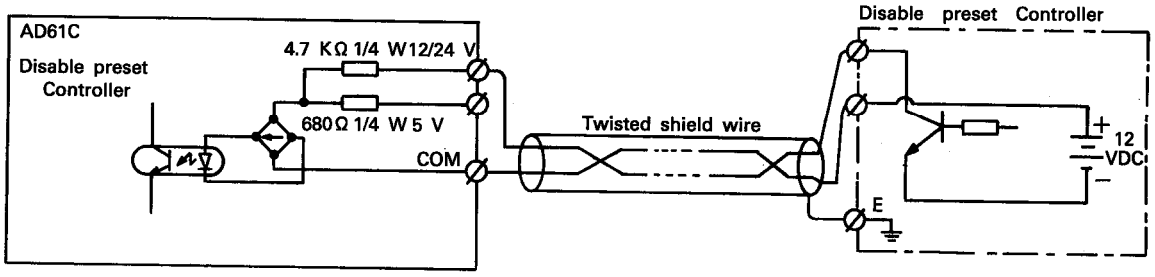
7.7.3 Voltage output pulse generator and wiring examples

(1) Connection of 5 VDC pulse generator



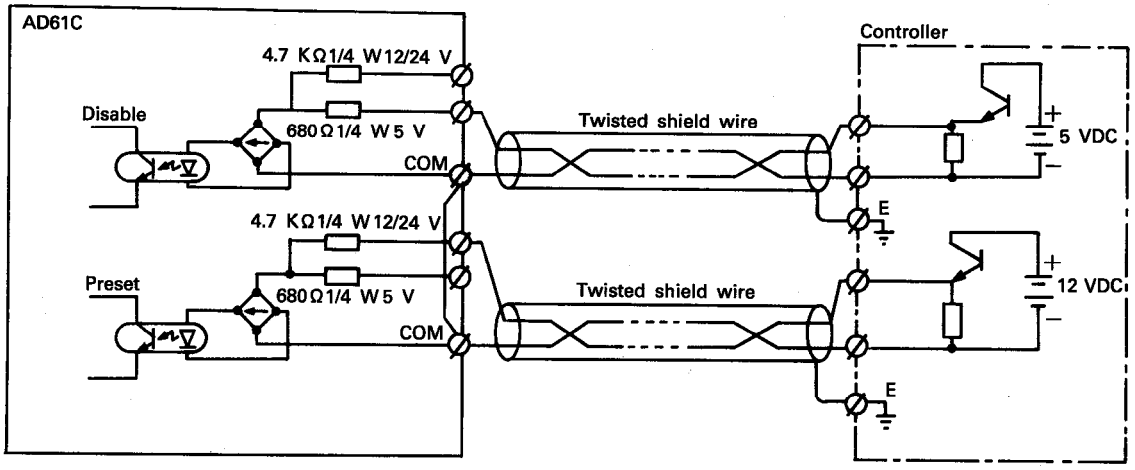
7.7.4 Wiring example for the connection of a controller to external input terminals (DIS, PRST)

(1) Connection of a controller to AD61C external input terminals (DIS, PRST)



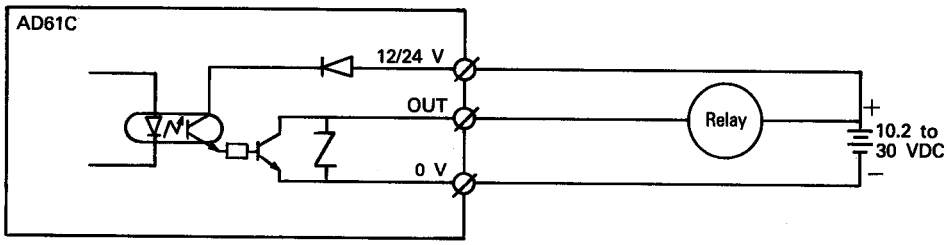
*1: The interface for disable input and preset input is the same.

(2) Connection of source load (voltage output type)



7.7.5 Wiring examples at external output (EQU) terminal

To use the EQU terminal, the internal photocoupler should be activated. For this purpose, 10.2 to 30 V external power is necessary. Connection methods are as follows:



8. TROUBLESHOOTING

8.1 Error Code List

(1) If an error occurs (RUN LED blinking) when executing FROM/TO instruction, the following error codes will be stored to buffer memory address 18. Correct as follows.

Error Code	Error and Cause	Corrective Action
100	(Read error) 1. When the FROM instruction is executed, head address number of buffer memory address is address 19 or larger. 2. An attempt is made to read words from the area exceeding address 19. 3. An attempt is made to read write only buffer memory.	Confirm the sequence program and correct.
101	(Write error) 1. When the TO instruction is executed, head address number of buffer memory address is address 19 or larger. 2. An attempt is made to write words to the area exceeding address 19. 3. An attempt is made to write to read only buffer memory.	Confirm the sequence program and correct.
102	Commands other than read/write have been received. Data has been rewritten due to noise.	Execute communication again. Take proper measures against noises.
103	Number of read/write specified words 0 has been received.	Execute communication again. Take proper measures against noises.
104	Data has been received when the FROM instruction is executed.	Execute communication again. Take proper measures against noises.
105	The number of words written and the number of words received are different when the TO instruction is executed.	Execute communication again. Take proper measures against noises.
1⬚0	Values other than 8 or 18 have been written to the mode register (addresses 0 and 7). [⬚ indicates the error-generating channel number.]	Confirm the sequence program and correct. (18 will be set as the default value.)

(a) When multiple errors occur, the AD61C stores the data error code of the first error detected by the AD61C and does not store subsequent errors.

(b) The error code is reset by writing 0 to buffer memory address 18. (Written values other than 0 are ignored.)

(c) When an error occurs, if error reset is executed without restoring the error, the AD61C restores normal state, the error code becomes 0, and the RUN LED is lit stopping blinking.

POINT

(1) When an AD61C error occurs, the A2CCPU stores a dedicated error code to special D.
(2) When an AD61C error occurs, the MINI-S3 Master Module stores the faulty station and AD61C error code to the buffer memory.

8.2 RUN LED is Flickering/OFF

(1) When flickering

Check Item	Corrective Action
Is there data which cannot not be written to or read from the AD61C?	Read the AD61C error code, confirm using the error code list in Section 8.1, and correct the sequence program.

(2) When OFF

Check Item	Corrective Action
Is the 24 VDC power supply charged?	• Turn ON the power supply.
Is the 24 VDC within the rated voltage?	• Set the voltage to 15.6 to 31.2 V.
Is the wiring correct?	• Check for cut wires and erroneous wiring and correct.
Is there a hardware error detected (watchdog timer error)?	• After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.) • If the LED is OFF, AD61C hardware is faulty. Consult Mitsubishi representative.

8.3 LINK RUN LED is OFF

Check Item	Corrective Action
Is the RUN LED lit?	• When the RUN LED is flickering or OFF, correct according to Section 8.2.
Is a hardware error detected?	• After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.) • If the LED is off, AD61C link hardware is faulty. Consult Mitsubishi representative.

8.4 LINK ERR.LED is ON

Check Item	Corrective Action
Is the communication cable wiring correct?	• Confirm whether link data communication is disabled due to cable wire breakage, terminal block faulty connections or wiring faults, and correct. • If the LED does not turn off when the wiring is correct, AD61C link hardware is faulty. Consult Mitsubishi representative.

8.5 Count Operations Do Not Execute

Check Item	Corrective Action
Are the RUN and LINK RUN LEDs lit?	• Correct according Sections 8.2 and 8.3 if they are flickering or OFF.
Is the LINK ERR. LED OFF?	• Correct according to Section 8.4 is the LINK ERR. LED is ON.
Is the external wiring of phases ϕA and B correct?	• Check the external wiring and correct.
Are phases ϕA and ϕB LEDs lit by directly applying voltage to the count input terminal?	• If yes, check the external wiring and pulse generator and correct. • If no, AD61C hardware is faulty. Consult Mitsubishi representative.
Is the enable LED ON?	• If it is OFF, correct the sequence program so that it is turned ON. (Turn OFF the disable input at external input terminal.)
Do the set AD61C station number and the station number specified by the sequence program coincidence?	• With the A2CCPU, coincidence the AD61C station number and program setting. • With the MINI-S3 master module, coincidence the program setting to the MINI-S3 master module buffer memory corresponding to the AD61C station number.
Is the phase specified to the AD61C buffer memory by the sequence program written with a correct value?	• Set the 1-phase specification of phase ϕA to the mode register or correct.
Are the ACPU/A2CCPU or MINI-S3 master module indicating an error?	• If it is the ACPU/A2CCPU, refer to the troubleshooting section of the manual of the PC CPU being used to recover correct operations. • If it is the MINI-S3 master module, return to normal operating state according to the troubleshooting section of the MINI-S3 master module manual.

(1) If counter operations cannot be executed even when the above check items are correct, AD61C hardware is faulty. Consult Mitsubishi representative.

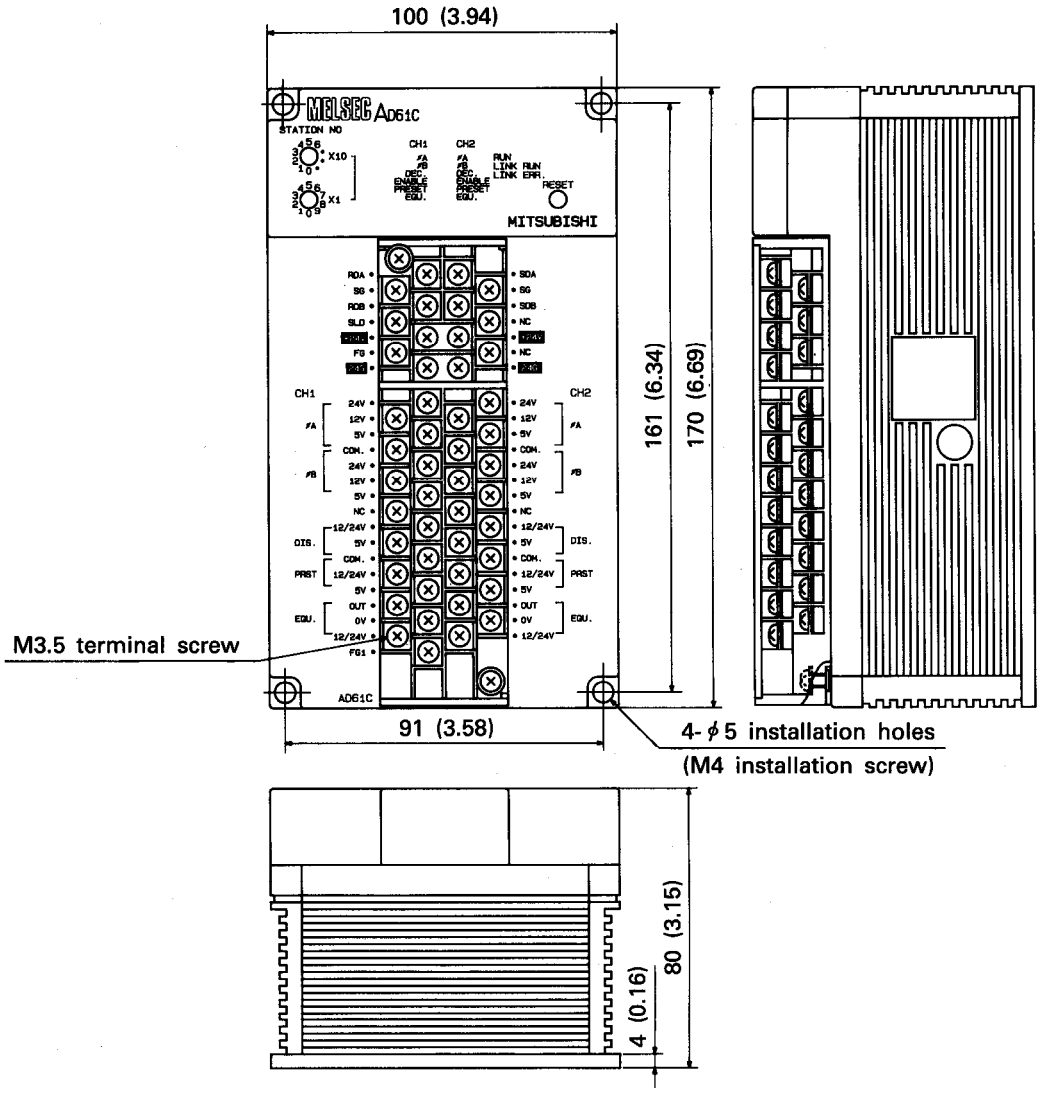
8.6 Count Value Is Incorrect

Check Item	Corrective Action
Is the counter input specification correct?	• Coincidence the counter input to the specification conditions in Section 2.2.
Are the sequence program data handled in 24-bit binary?	• Correct the sequence program so that its data can be handled in 24-bit binary.
Is the phase setting for the sequence program input pulses correct?	• For 1-phase inputs, set 8 to the mode register and for 2-phase inputs, set 18. (The default value is 18 for 2-phase inputs)
Is twisted shield wire used for counter input wiring?	• Use twisted shield wire for counter input wiring.
Are spurious counter values related to the operation of other equipment?	• Separate wiring of related equipment.
Does noise come in through the ground of the AD61C?	• Disconnect the AD61C from the ground. • If the case of the AD61C contacts the ground, separate it from the ground.
Have adequate measures been taken against noise in the panel?	• Provide CR surge suppression to magnetic switches, etc.
Is sufficient distance provided between heavy current equipment and counter input line?	• Independently wire counter input line. Separate wire in panel 150 mm (5.91 in.) or more from power line.
Are counter values the same by providing the same count inputs to CH1 and CH2?	• If not, AD61C hardware is faulty. Consult Mitsubishi representative.
If the counter values are the same by providing the same count inputs to CH1 and CH2, do the pulse input waveform, rise, and fall conform to the specifications?	• Monitor and confirm the input waveform using a synchroscope. If the rise and fall are outside the specified value, resulting in a faulty waveform, correct the waveform.

(1) If counter operations cannot be executed correctly even when the above check items are correct, AD61C hardware is faulty. Consult Mitsubishi representative.

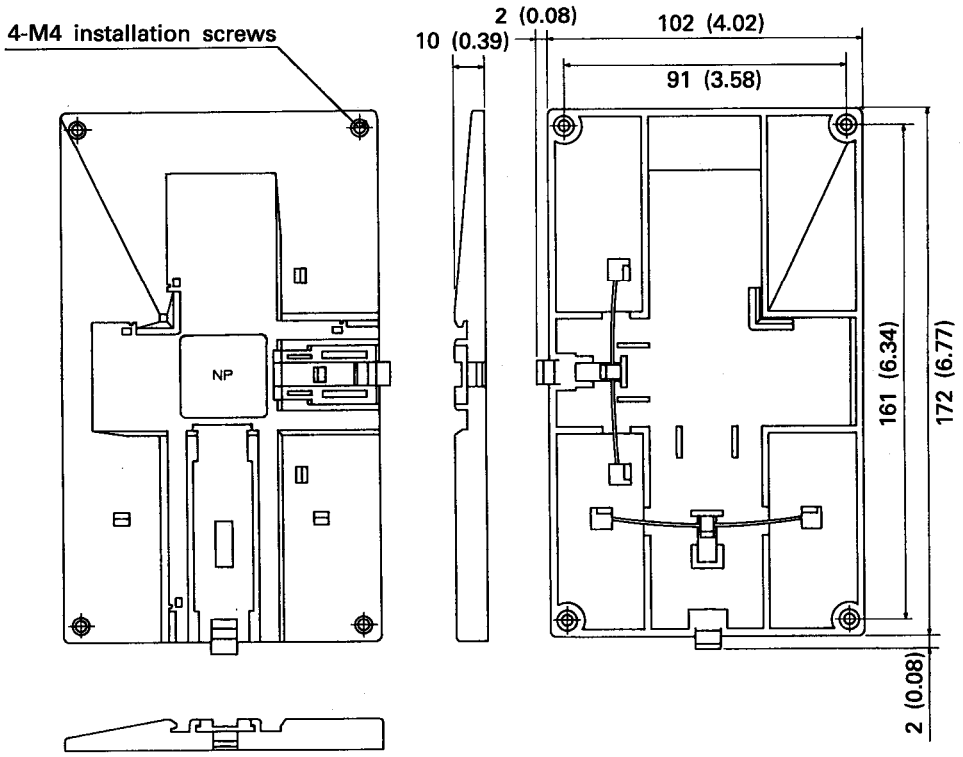
APPENDICES

APPENDIX 1 Dimensions



Unit: mm (in)

APPENDIX 2 DIN Adapter Dimensions



Unit: mm (in)

APP

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.
However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.
Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.
(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.
1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.
(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation of damages caused by any cause found not to be the responsibility of Mitsubishi, loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products, special damages and secondary damages whether foreseeable or not , compensation for accidents, and compensation for damages to products other than Mitsubishi products, replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.
(2) The Mitsubishi programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or Public service purposes shall be excluded from the programmable logic controller applications.
In addition, applications in which human life or property that could be greatly affected, such as in aircraft, medical applications, incineration and fuel devices, manned transportation, equipment for recreation and amusement, and safety devices, shall also be excluded from the programmable logic controller range of applications.
However, in certain cases, some applications may be possible, providing the user consults their local Mitsubishi representative outlining the special requirements of the project, and providing that all parties concerned agree to the special circumstances, solely at the users discretion.

High Speed Counting Module Type AD61C

User's Manual

MODEL	AD61C-USERS-E
MODEL CODE	13J779
IB(NA)-66246-B(0411)MEE	

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : 1-8-12, OFFICE TOWER Z 14F HARUMI CHUO-KU 104-6212,JAPAN
NAGOYA WORKS : 1-14 , YADA-MINAMI 5-CHOME , HIGASHI-KU, NAGOYA , JAPAN

When exported from Japan, this manual does not require application to the Ministry of Economy, Trade and Industry for service transaction permission.

Specifications subject to change without notice.